Introduction To Semiconductor Manufacturing Technology

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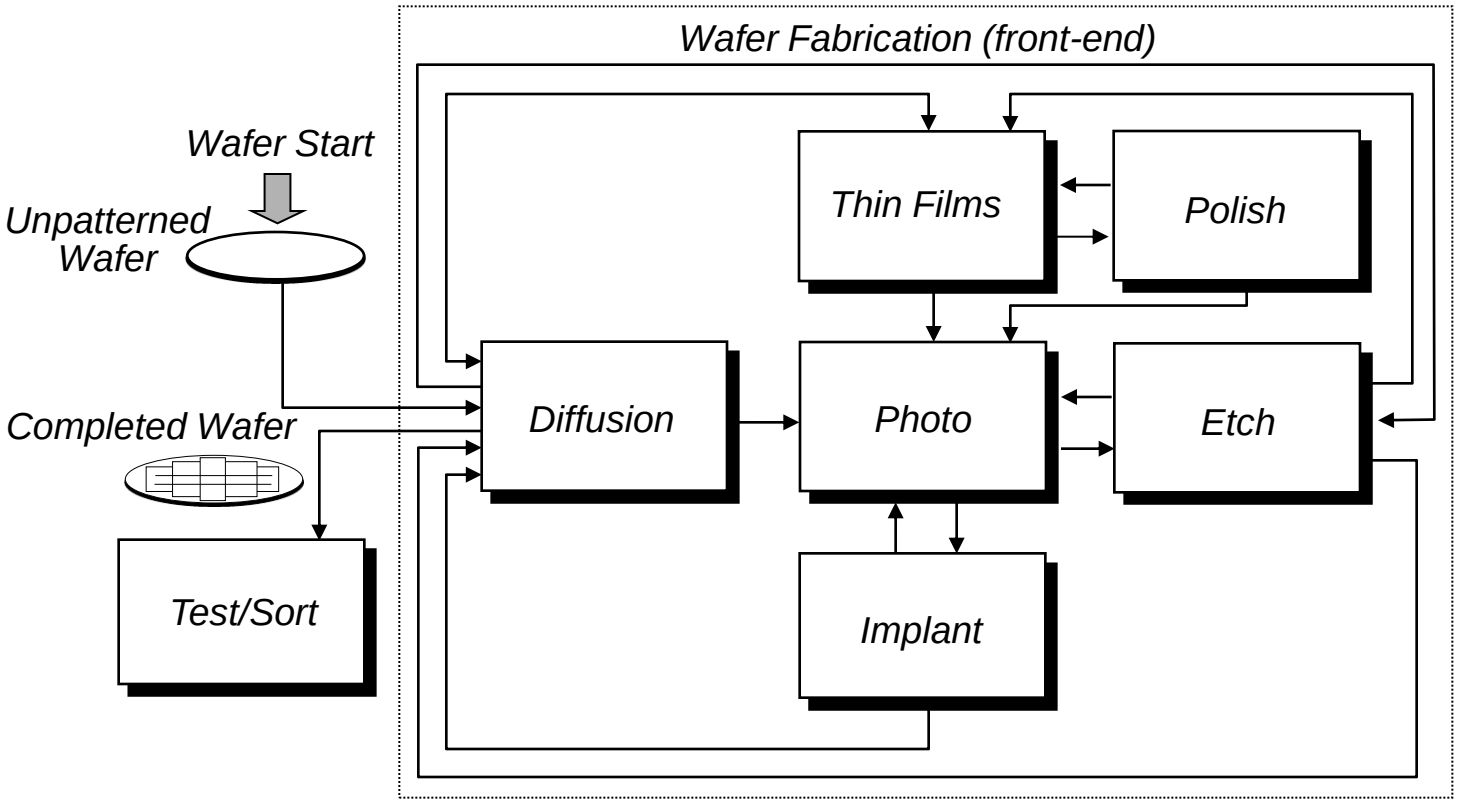
CMOS Process Flow

- Overview of Areas in a Wafer Fab
  - Diffusion (oxidation, deposition and doping)
  - Photolithography
  - Etch
  - Ion Implant
  - Thin Films
  - Polish
- CMOS Manufacturing Steps
- Parametric Testing
- 6~8 weeks involve 350-step

Model of Typical Wafer Flow in a Sub-Micron CMOS IC Fab



6 major production areas

Clean: Types of Contamination and The Problems They Cause

- Particles
- Metallic Impurities
- Organic Contamination
- Native Oxides
- Electrostatic Discharge

- Contamination often leads to a defective chip. Killer defects are those causes of failure where the chip on the wafer fails during electrical test.
- It is estimated that 80% of all chip failure are due to killer defects from contamination.

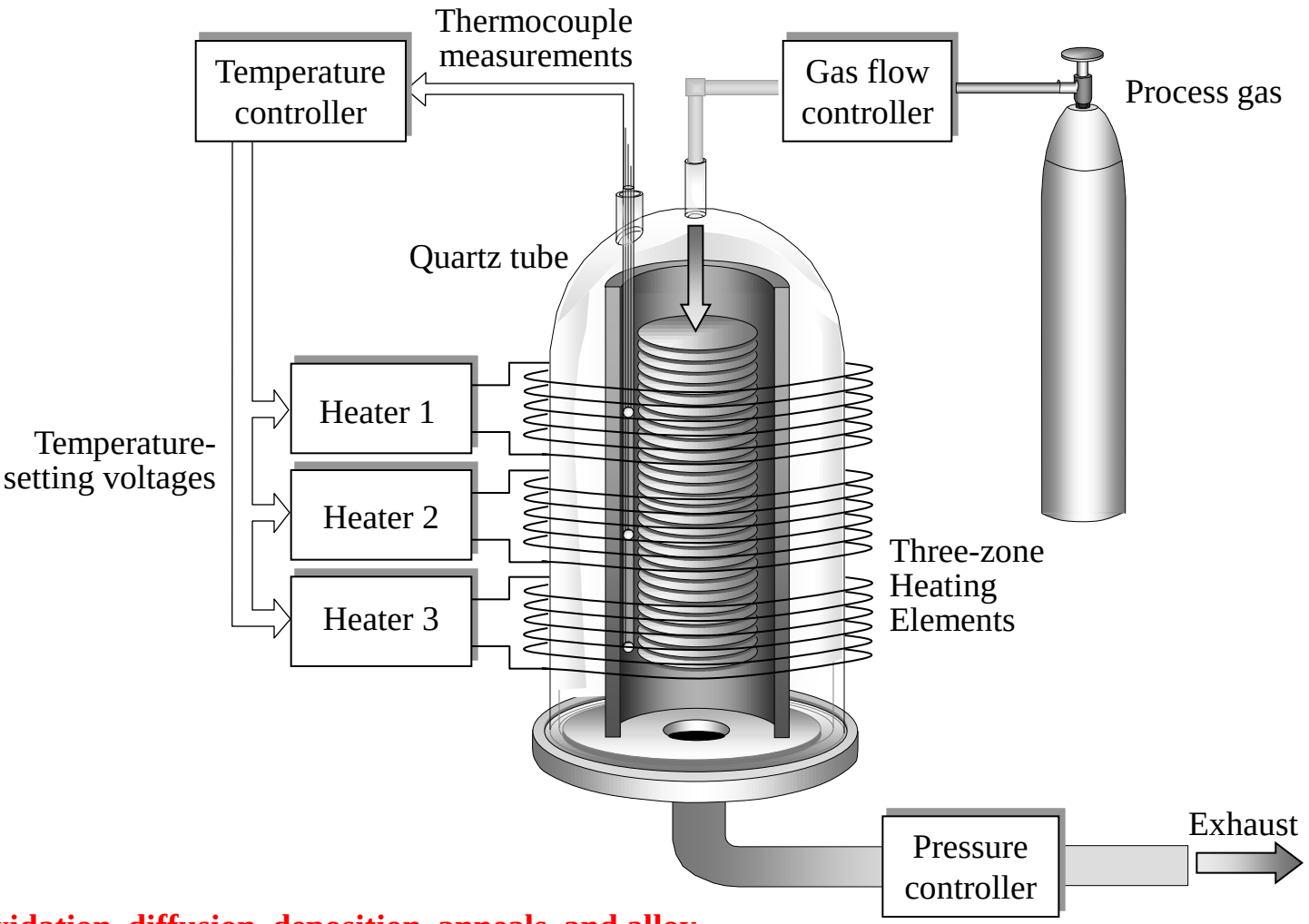
Wafer Wet-Cleaning Chemicals

Contaminant	Name	Chemical Mixture Description (all Cleans are followed by a DI Water Rinse)	Chemicals
Particles	Piranha (SPM)	▪ Sulfuric acid/hydrogen peroxide/DI water	$H_2SO_4/H_2O_2/H_2O$
	SC-1 (APM)	• Ammonium hydroxide/hydrogen peroxide/DI water	$NH_4OH/H_2O_2/H_2O$
Organics	SC-1 (APM)	• Ammonium hydroxide/hydrogen peroxide/DI water	$NH_4OH/H_2O_2/H_2O$
Metallics **(not Cu)**	SC-2 (HPM)	• Hydrochloric acid/hydrogen peroxide/DI water	$HCl/H_2O_2/H_2O$
	Piranha (SPM)	▪ Sulfuric acid/hydrogen peroxide/DI water	H_2SO_4/H_2O_2
	DHF	• Hydrofluoric acid/water solution (will not remove copper)	HF/H_2O
Native Oxides	DHF	• Hydrofluoric acid/water solution (will not remove copper)	HF/H_2O
	BHF	• Buffered hydrofluoric acid	$NH_4F/HF/H_2O$

Typical Wafer Wet-Cleaning Sequence

Cleaning Step	What it Cleans
H_2SO_4/H_2O_2 (piranha)	**Organics & metals**
UPW rinse (ultrapure water)	Rinse
HF/H_2O (dilute HF)	Native oxides
UPW rinse	Rinse
$NH_4OH/H_2O_2/H_2O$ (SC-1)	**Particles**
UPW rinse	Rinse
HF/H_2O	Native oxides
UPW rinse	Rinse
$HCl/H_2O_2/H_2O$ (SC-2)	**Metals**
UPW rinse	Rinse
HF/H_2O	Native oxides
UPW rinse	Rinse
Drying	Dry

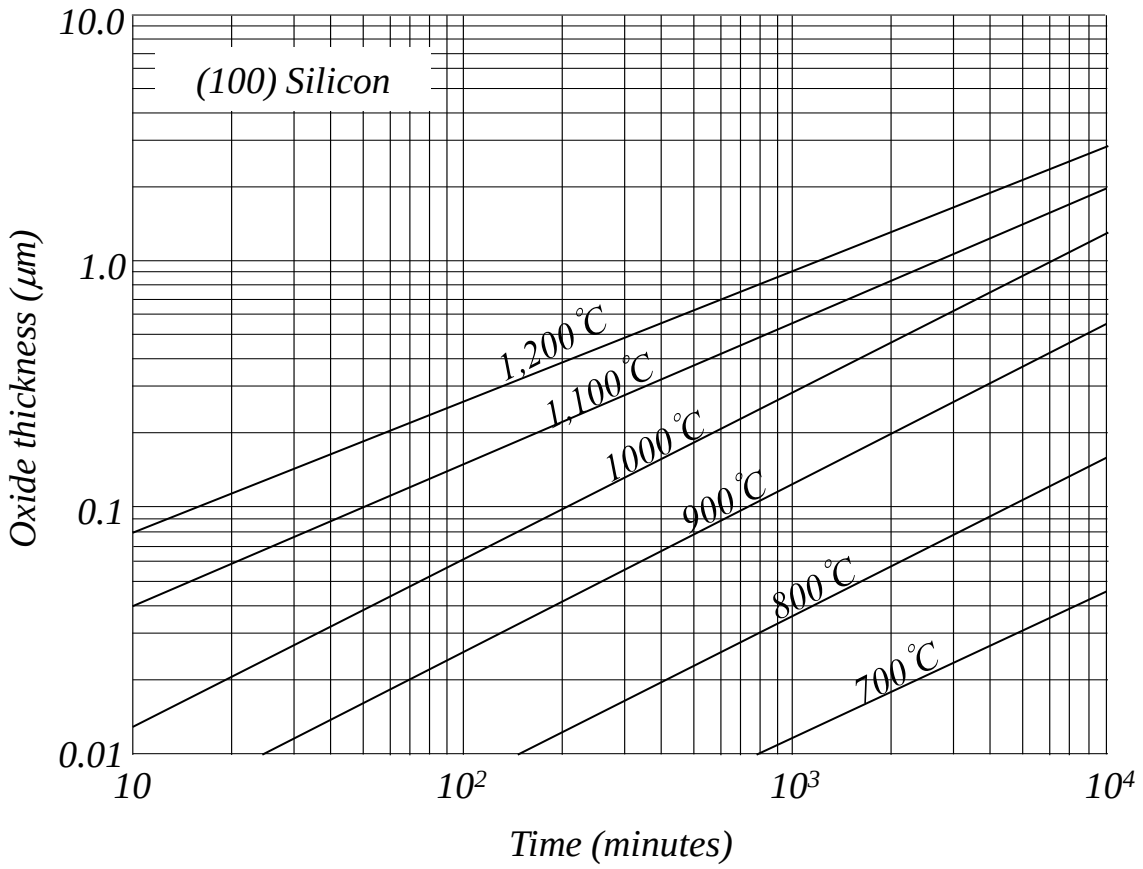
Diffusion: Simplified Schematic of High-Temperature Furnace



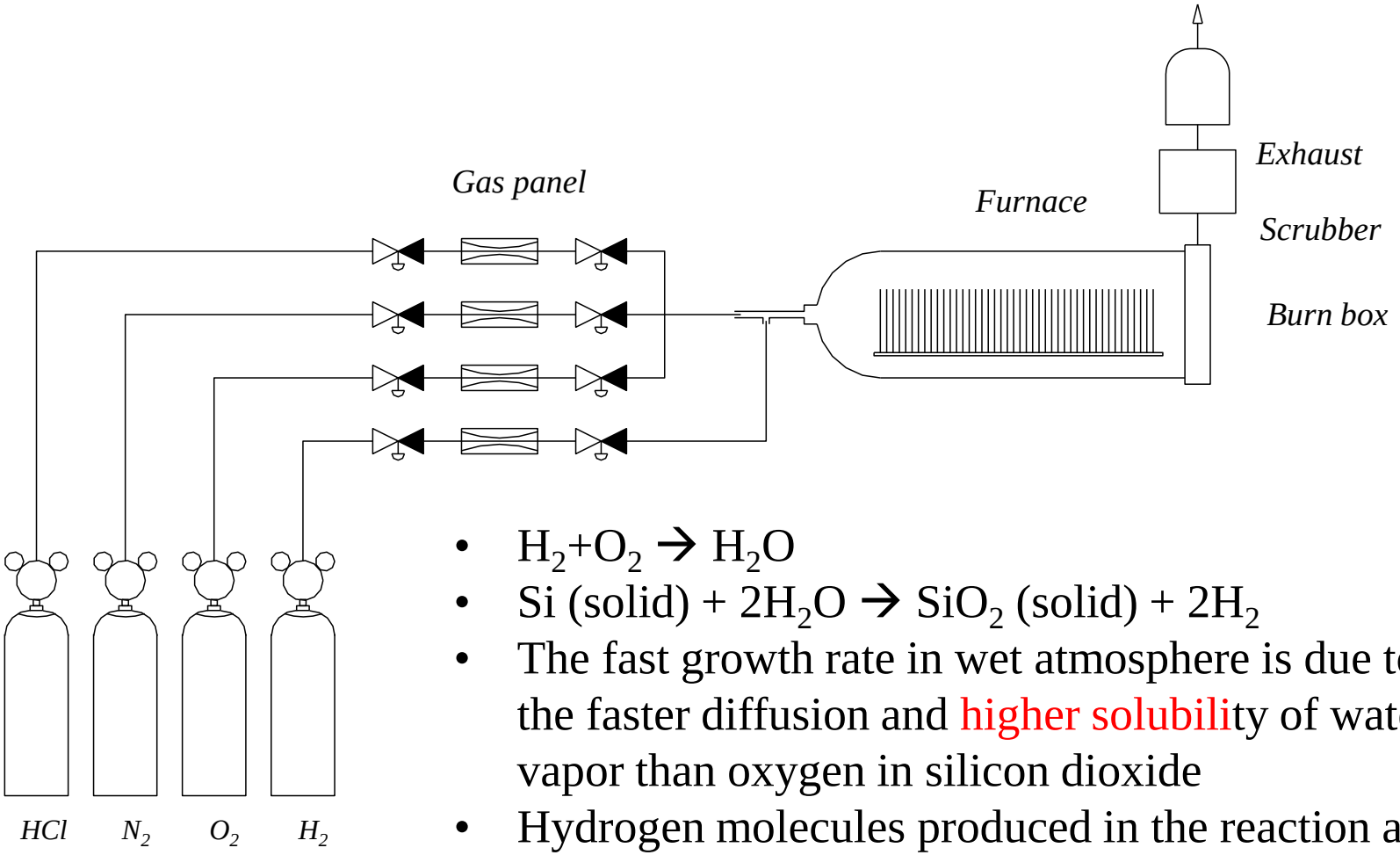
Can do : oxidation, diffusion, deposition, anneals, and alloy

Dry Oxidation Time (Minutes)

$$Si\ (solid) + O_2\ (gas) \rightarrow SiO_2\ (solid)$$

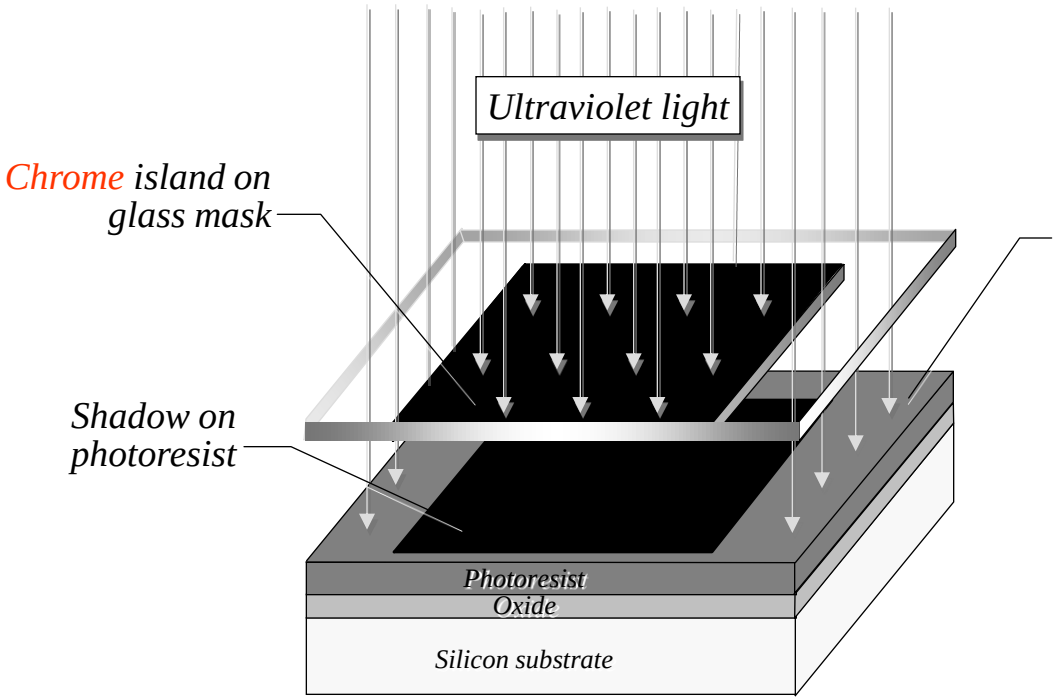


Wet Oxygen Oxidation

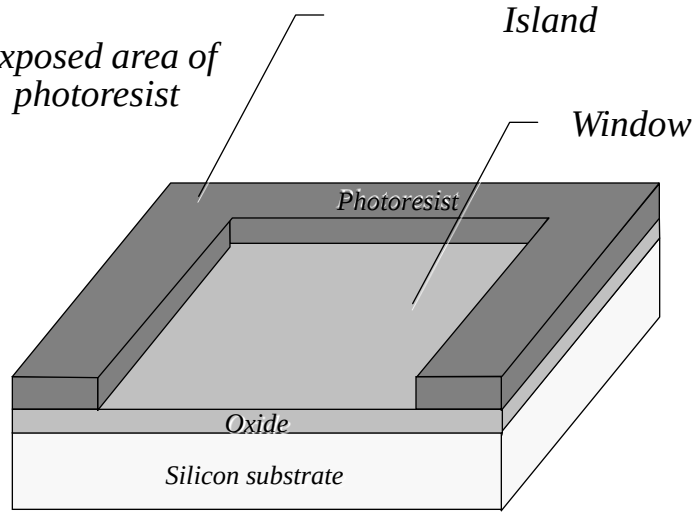


- $H_2+O_2 \rightarrow H_2O$
- Si (solid) + $2H_2O \rightarrow SiO_2$ (solid) + $2H_2$
- The fast growth rate in wet atmosphere is due to the faster diffusion and higher solubility of water vapor than oxygen in silicon dioxide
- Hydrogen molecules produced in the reaction are trapped in oxide, less dense, using heating (annealing) to improve.

Negative **Lithography**

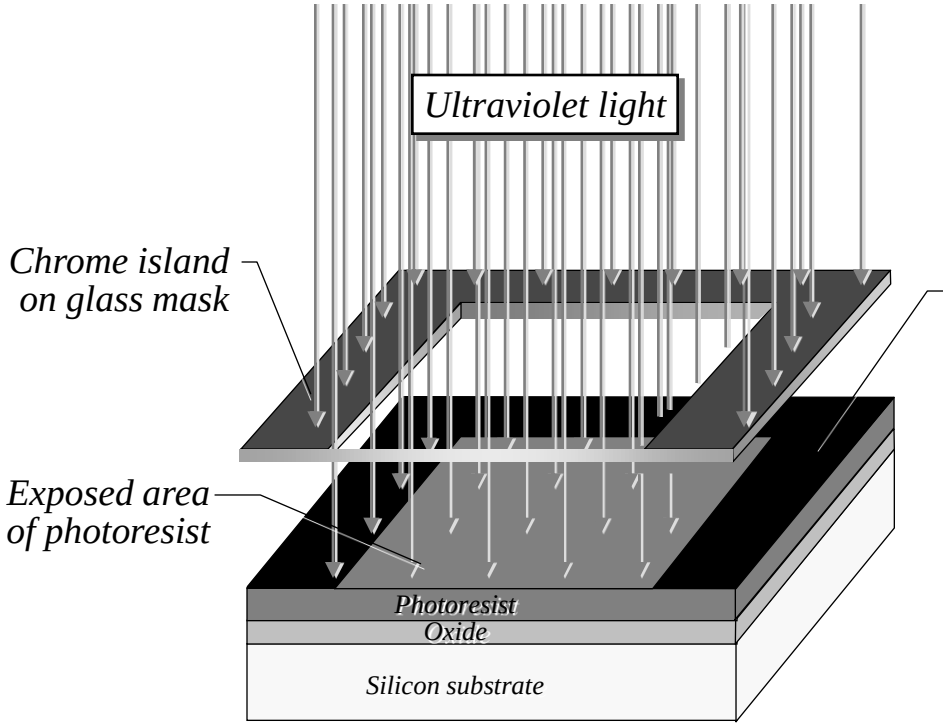


- Areas exposed to light become crosslinked and resist the developer chemical.

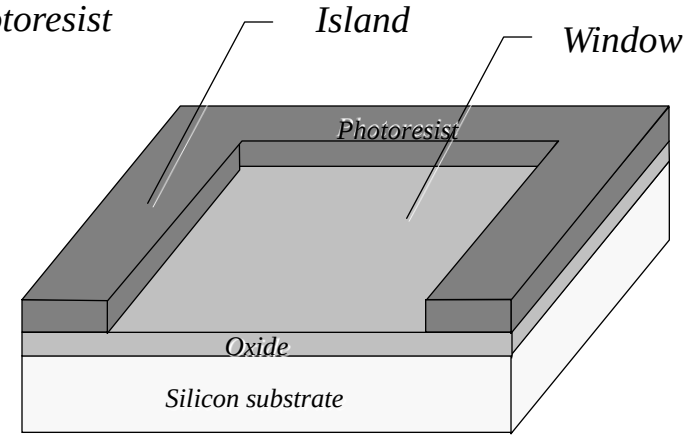


Resulting pattern after the resist is developed.

Positive Lithography

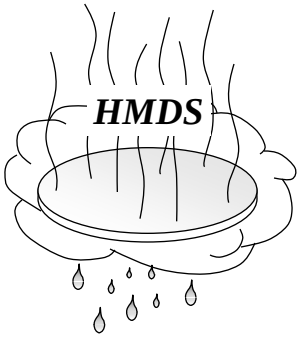


Areas exposed to light are dissolved.

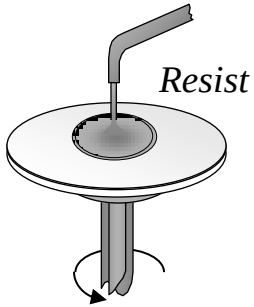


Resulting pattern after the resist is developed.

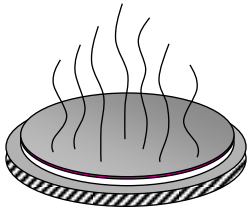
Eight Steps of Photolithography



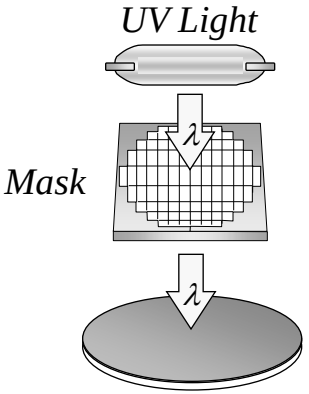
1) Vapor prime



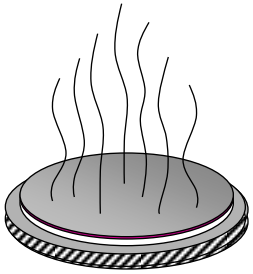
2) Spin coat



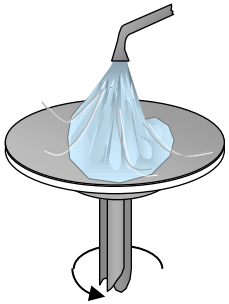
3) Soft bake



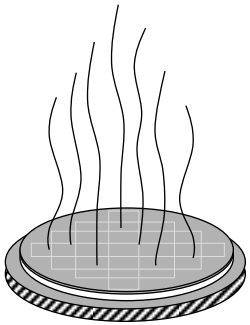
4) Alignment and Exposure



5) Post-exposure bake



6) Develop



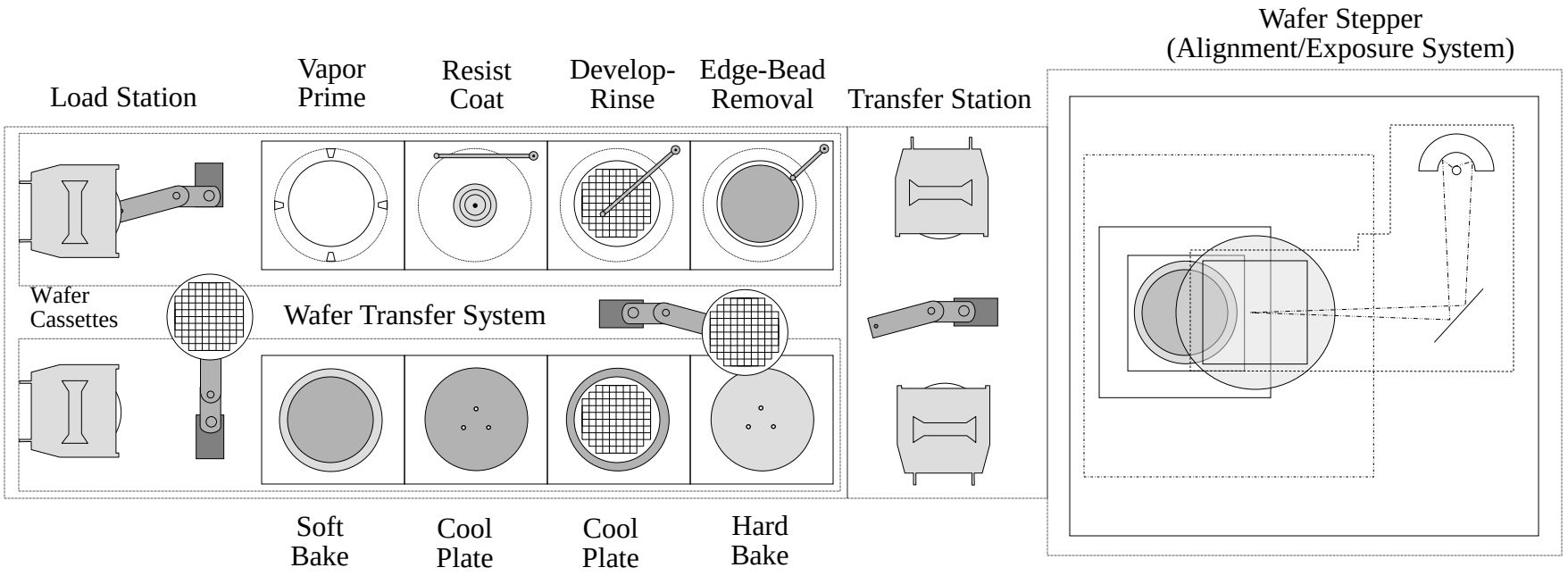
7) Hard bake

8) Develop inspect

Photolithography Bay in a Sub-micron Wafer Fab

- It is to photograph the image of a circuit pattern onto the photoresist that coats the wafer surface.
- Yellow fluorescent does not affect photoresist, but sensitive to UV

Simplified Schematic of a Photolithography Processing Module



Note: **wafers flow from photolithography into only two other areas: <u>etch</u> and <u>ion</u> <u>implant</u>**

Etch: Dissociation

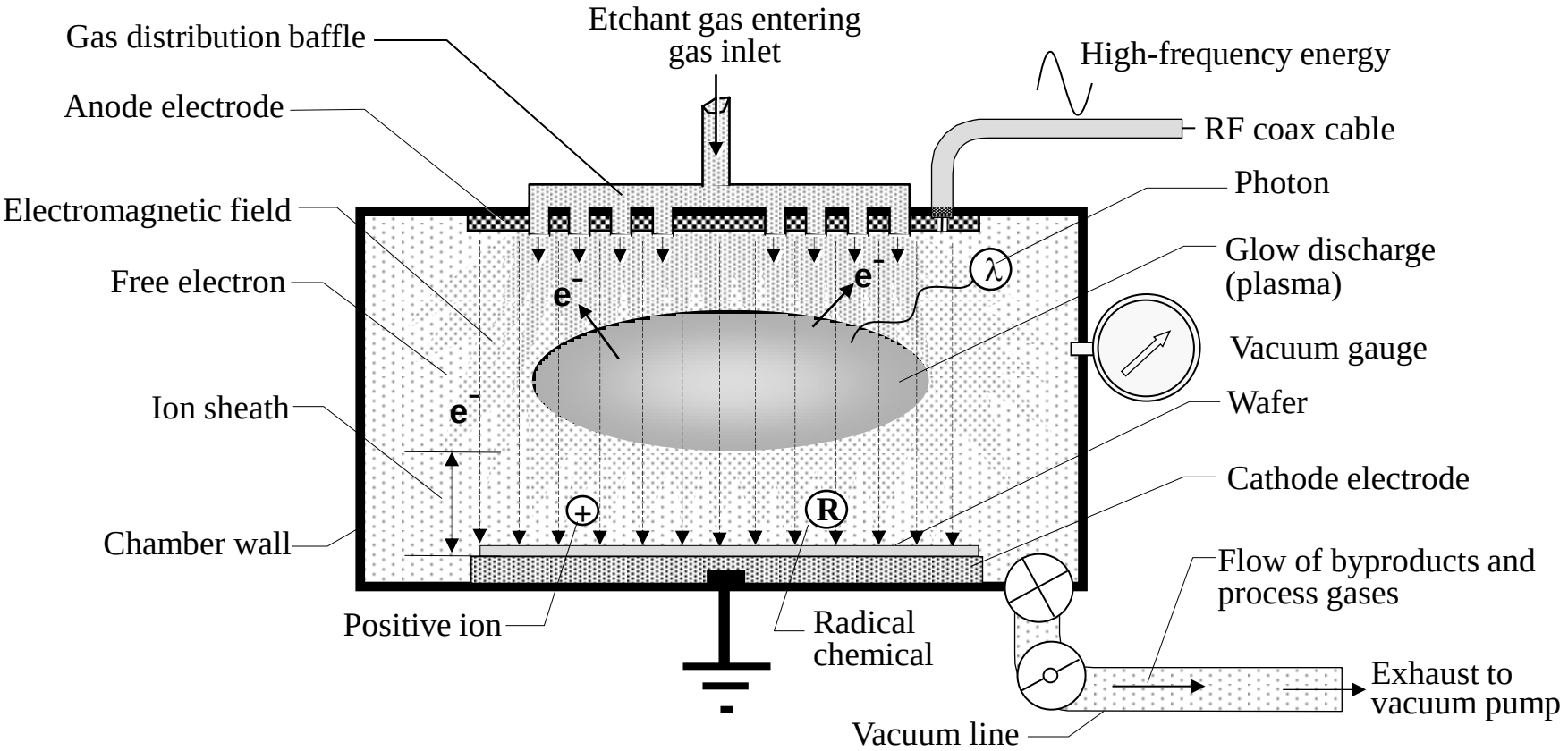
- Electron collides with a molecule, it can break the chemical bond and generate free radicals:

$$e + AB \longrightarrow A + B + e$$

- Free radicals have at least one unpaired electron and are chemically very reactive.
- Increasing chemical reaction rate
- Very important for both etch and CVD.

Simplified Schematic of Dry Plasma Etcher

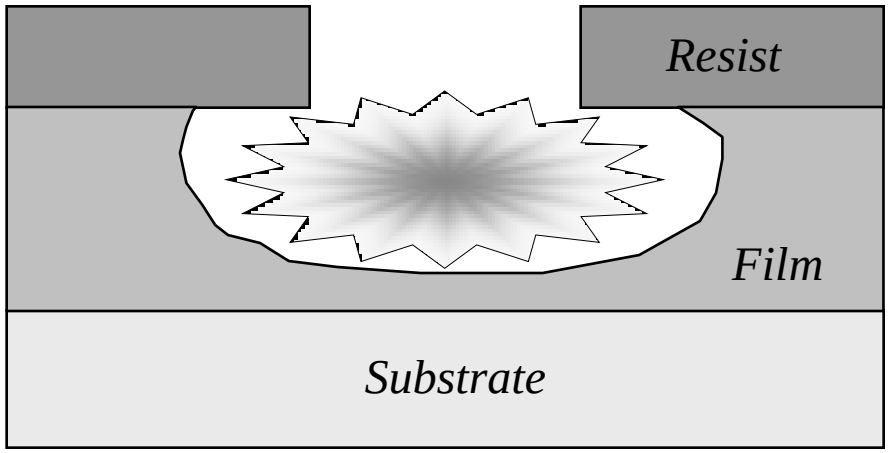
- The etch process creates a permanent pattern on the wafer in areas not protected by the photoresist pattern
- Including: dry etching, wet etching and photoresist stripper
- After dry etching: photoresist stripper + wet cleaning



Wet Chemical Isotropic Etch

- Etch profile refers to the shape of the sidewall of the etched feature
- Isotropic etch profile leads to a undercutting, results in an undesirable loss of the linewidth

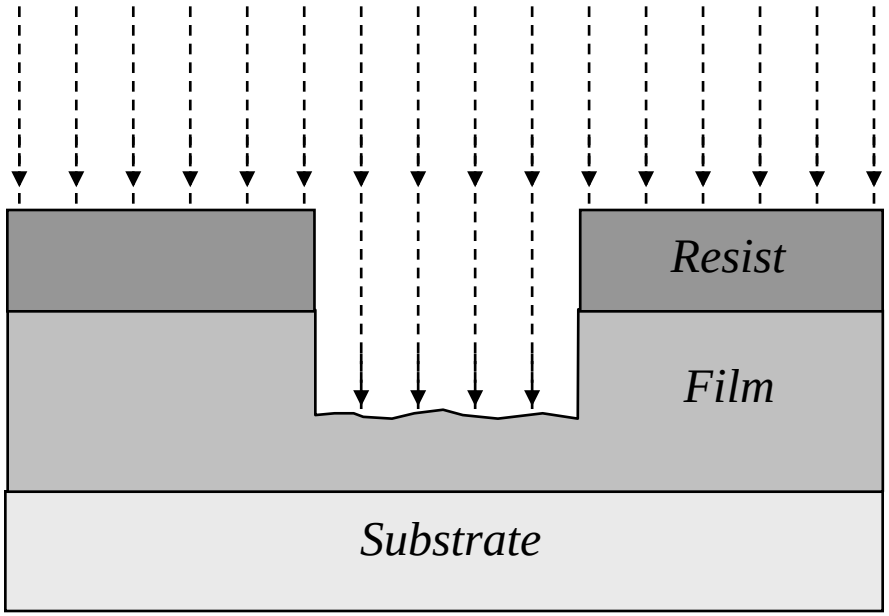
Isotropic etch - etches in all directions at the same rate



Anisotropic Etch with Vertical Etch Profile

- The rate of etching is on only one direction perpendicular to the wafer surface
- There is very little lateral etching activity
- This leaves vertical sidewalls, permitting a higher packing density of etched features on the chip
- With smaller geometries, the etch profiles have higher aspect ratios
- It is difficult to get etchant chemicals in and reaction by-products out of the high-aspect ratio openings

Anisotropic etch - etches in only one direction



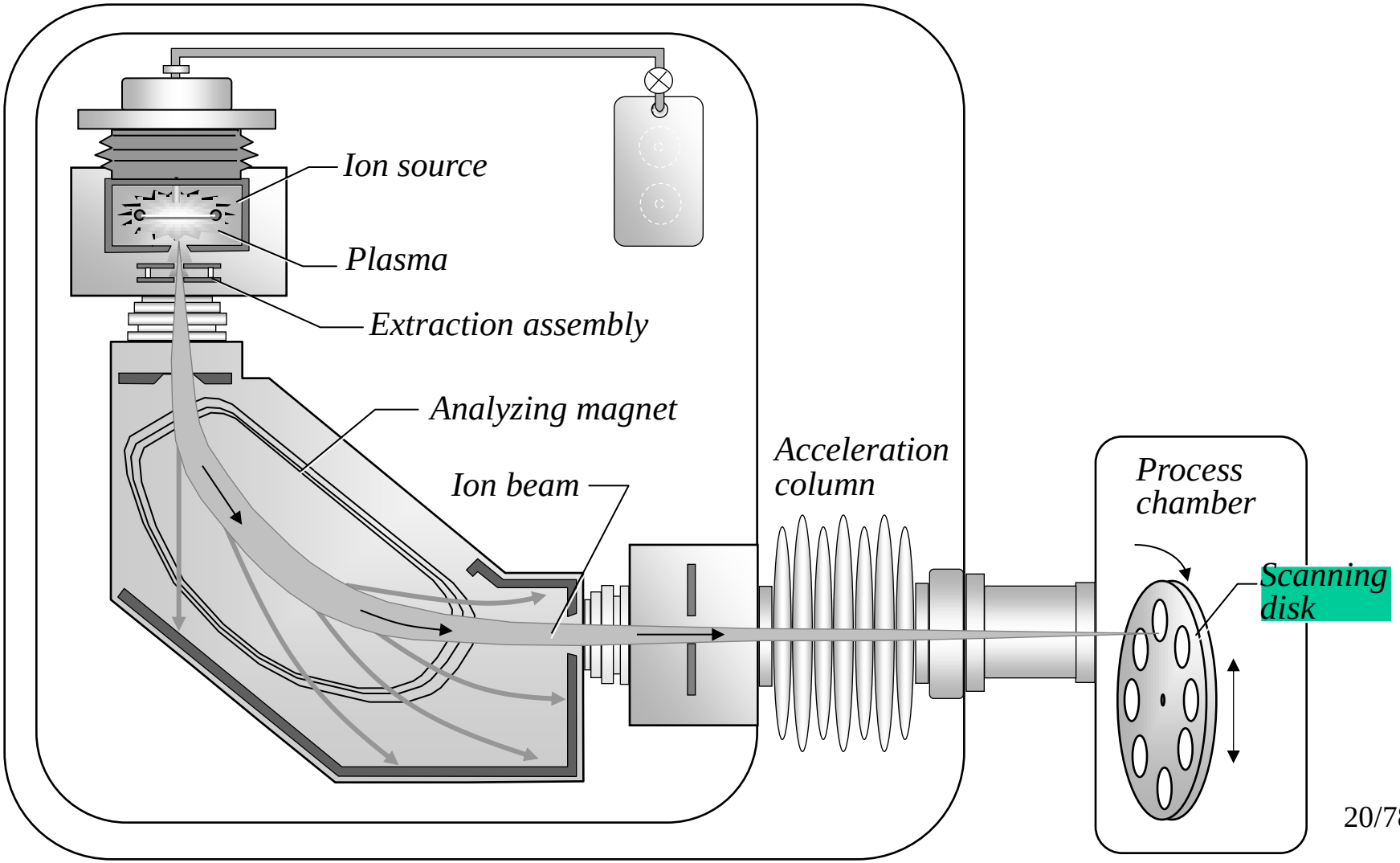
Implantation: Common Dopants Used in Semiconductor Manufacturing

- Doping is the introduction of a dopant into the crystal structure of a semiconductor material to modify its electronic properties
- Dopants are referred to as impurities
- Two techniques: thermal diffusion and ion implantation (dominant)

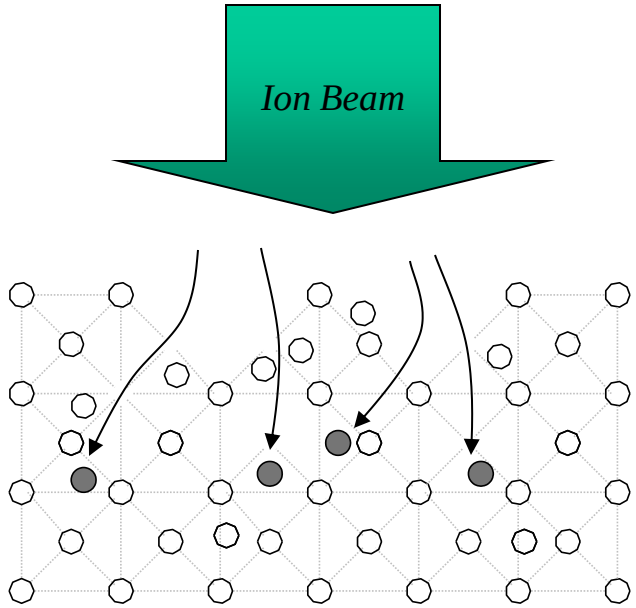
Acceptor Dopant Group IIIA (P-Type)		**Semiconductor Group IVA**		**Donor Dopant Group VA (N-Type)**	
Element	**Atomic Number**	**Element**	**Atomic Number**	**Element**	**Atomic Number**
Boron (B)	**5**	Carbon	6	Nitrogen	7
Aluminum	13	Silicon (Si)	14	**Phosphorus (P)**	**15**
Gallium	31	Germanium	32	**Arsenic (As)**	**33**
Indium	49	Tin	50	**Antimony**	**51**

General Schematic of an Ion Implanter

- *Ion source: positive charge*
- *Extraction assembly: extract ions*
- *Mass Analyzer: form a beam of the desired dopant ions*
- *Acceleration column: to attain a high velocity*

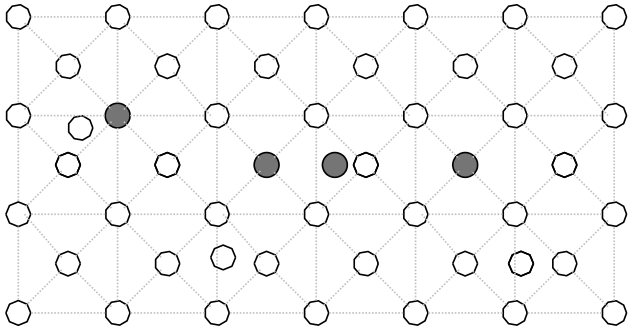


Annealing of Silicon Crystal



a) Damaged Si lattice during implant

Repaired Si lattice structure and activated dopant-silicon bonds

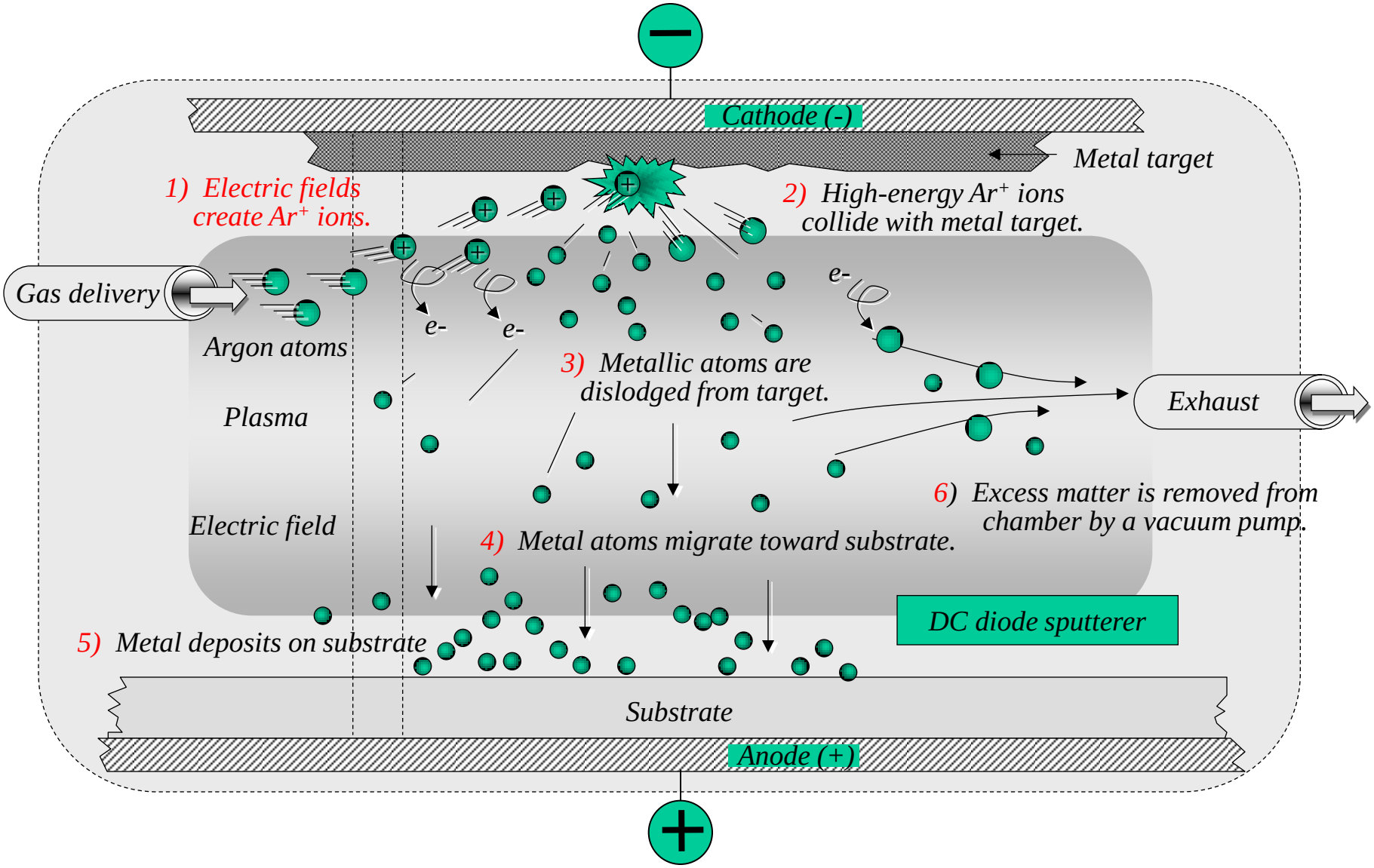


b) Si lattice after annealing

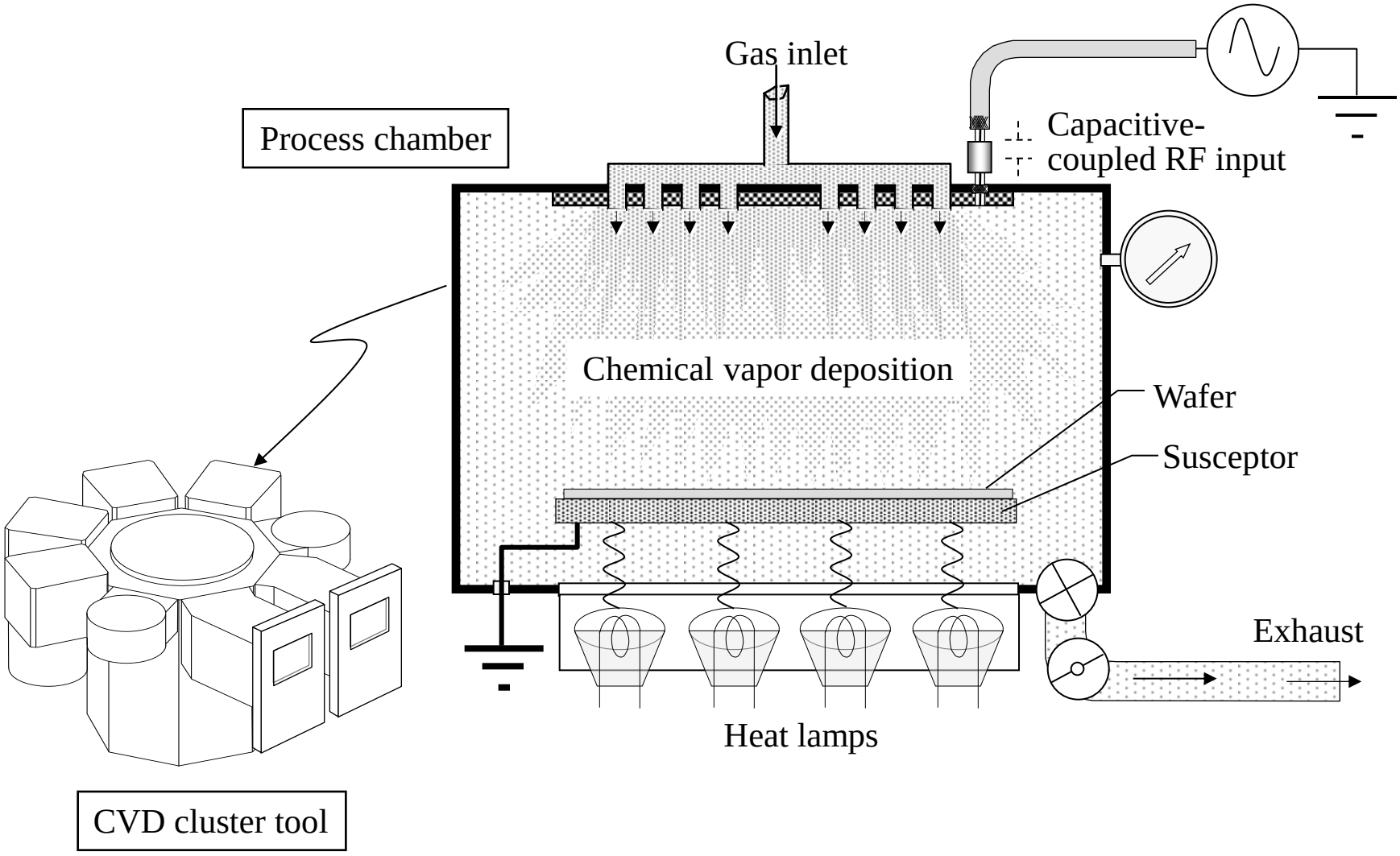
- Using Furnace or RTA, hot-wall furnace using high temperature causes extensive dopant diffusion and is undesirable
- RTA minimizes a phenomenon known as transient enhanced diffusion, to achieve acceptable junction depth control in shallow implants (~150°C/sec)

Thin Film Metallization Bay

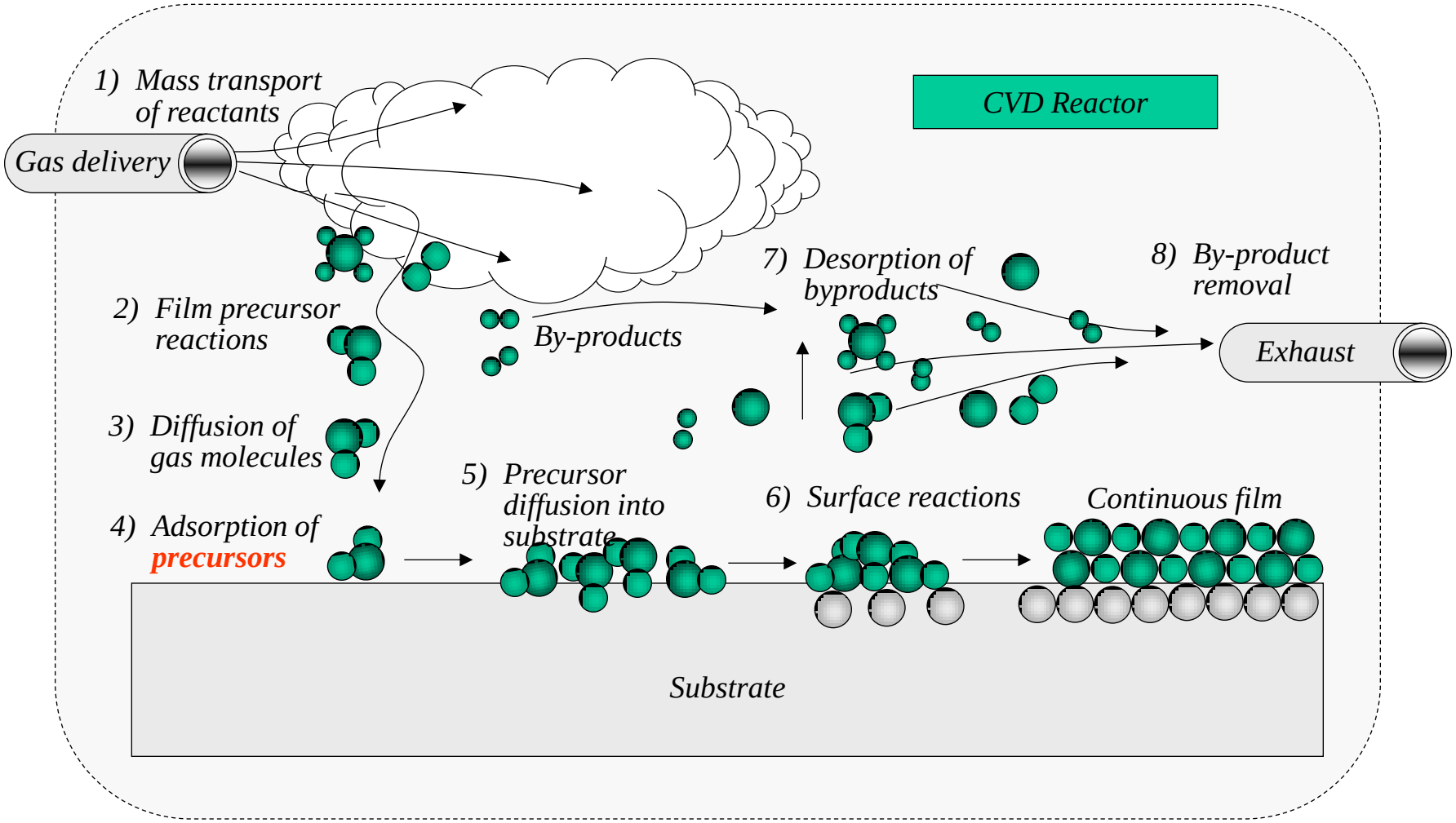
Simple Parallel Plate DC Diode Sputtering System



Simplified Schematics of CVD Processing System



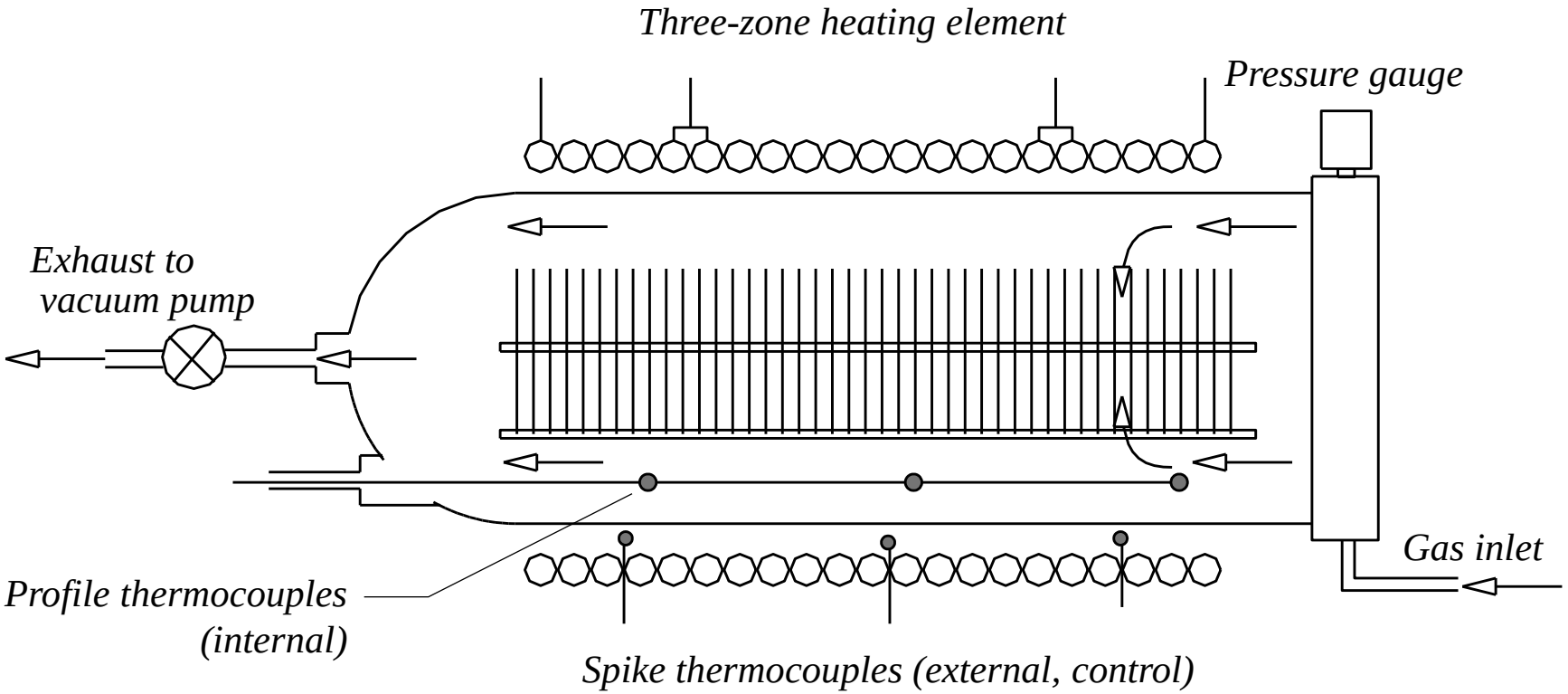
Schematic of CVD Transport and Reaction 8 Steps



CVD Reaction

- Take place on wafer surface: heterogeneous reaction (surface catalyzed).
- Homogeneous reaction: above surface (gas reaction), which is poor adhesion, low-density with high defects
- $SiH_4 \rightarrow SiH_2 + H_2$ (SiH_2 is precursor, it is pyrolysis)
- CVD reaction steps are sequential, the slowest step defines the bottleneck

LPCVD Reaction Chamber for Deposition of Oxides, Nitrides, or Polysilicon



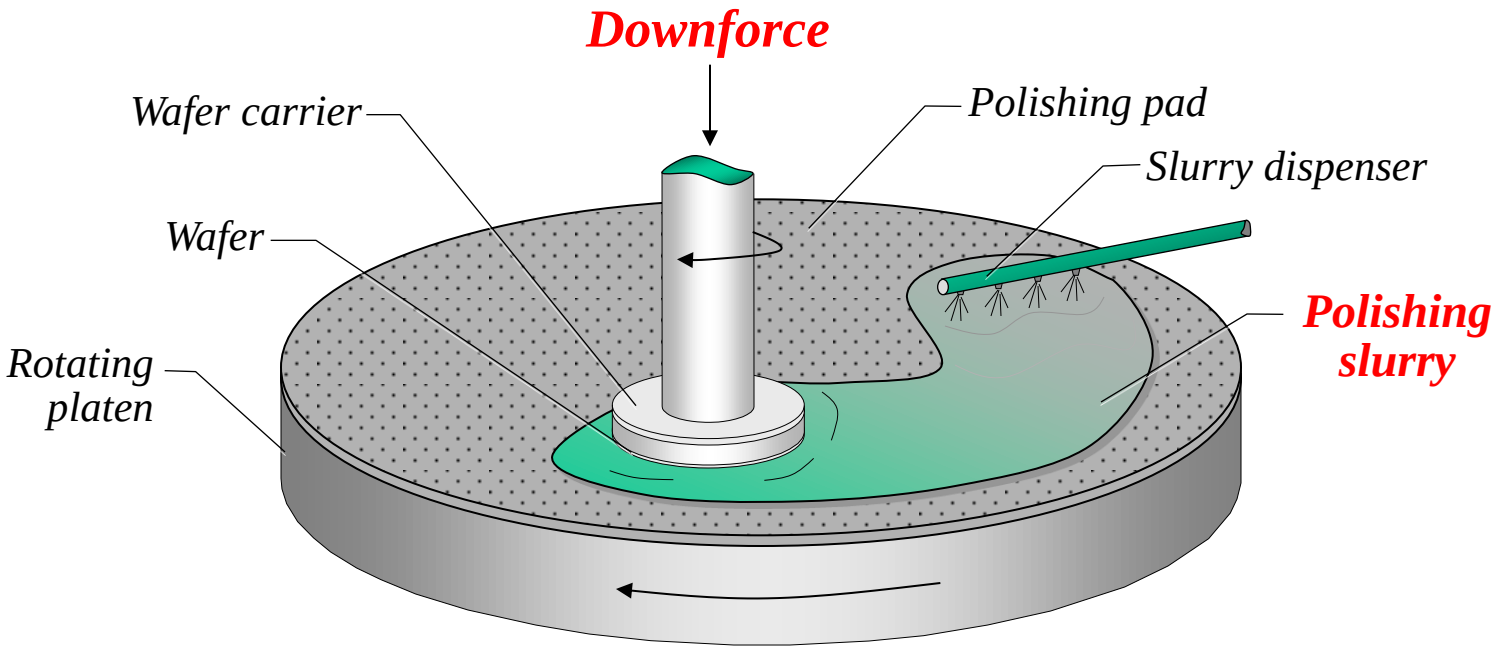
- Limited by surface reaction, flow condition is not important
- Films are uniformly deposited on a large number of wafer surface as long as the temperature is tightly controlled
- Conformal film coverage on the wafer
- Low growth rate than APCVD and need routine maintenance
- In-situ clean, using ClF_3 or NF_3
- $3SiCl2H2 + 4NH3 \rightarrow Si3N4 + 6HCl + 6H2$

Polish Bay in a Sub-micron Wafer Fab

- Chemical mechanical planarization (CMP) process is to planarize the top surface of the wafer by lowering the high topography to be level with the lower surface area of the wafer
- It combines chemical etching and mechanical abrading to remove layer

Schematic of Chemical Mechanical Planarization (CMP)

Step height: etchback ~ 7000Å vs. CMP ~ 50Å



- CMP achieves wafer planarity by removing high features on the surface more quickly relative to the low feature (high pressure by Preston's eq.)
- Both metal and dielectric layers can be removed

Biasing Circuit for an NMOS Transistor

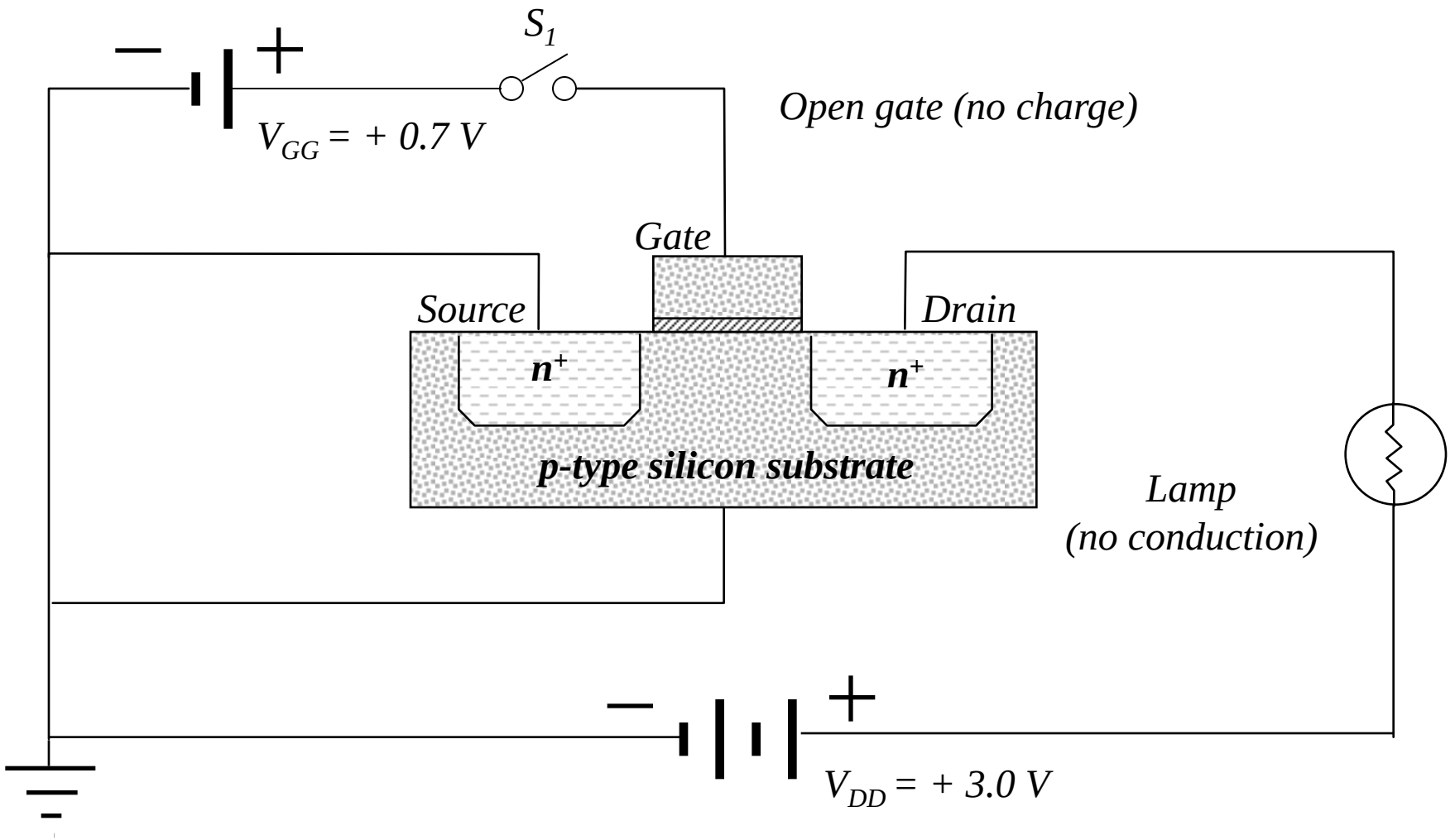
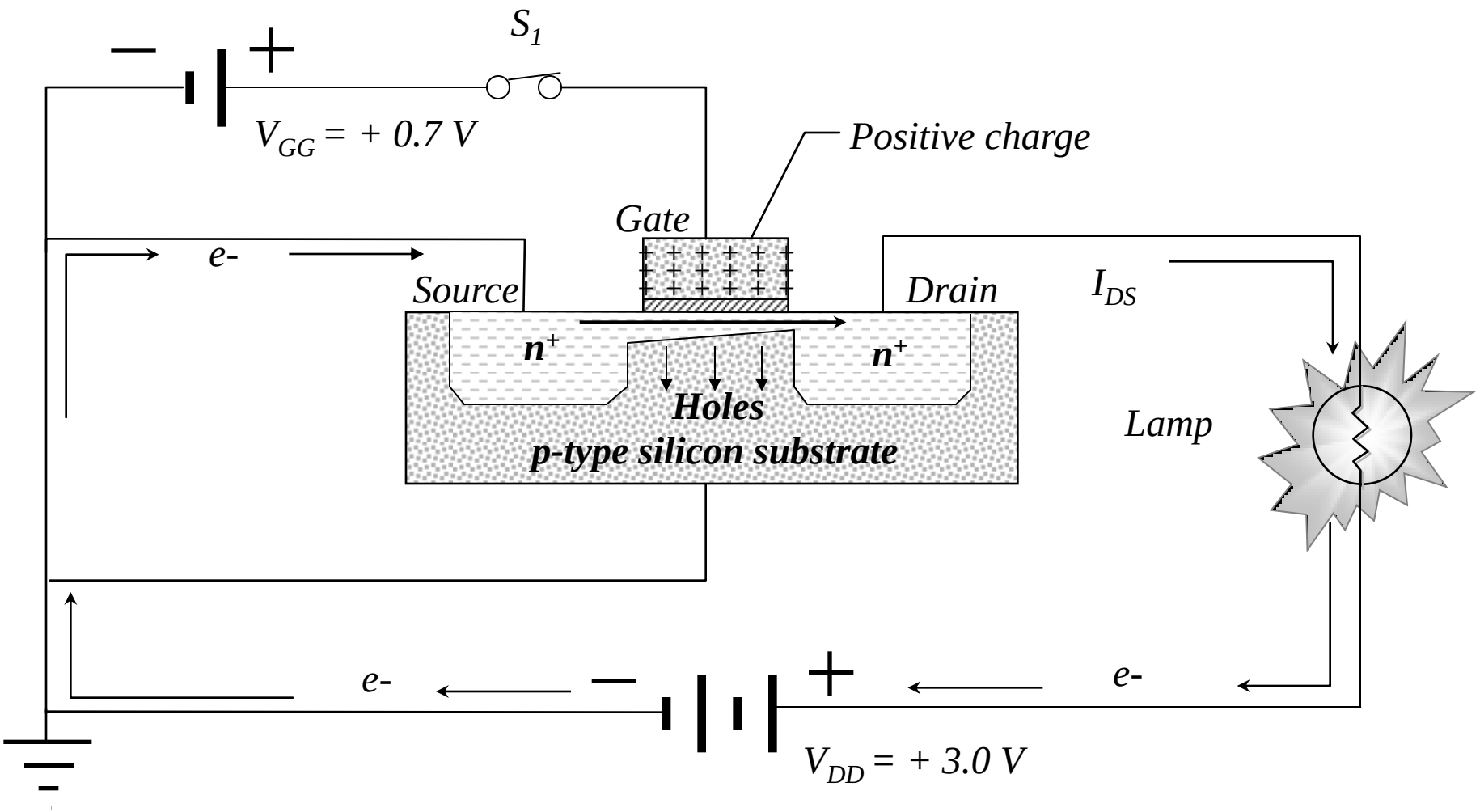
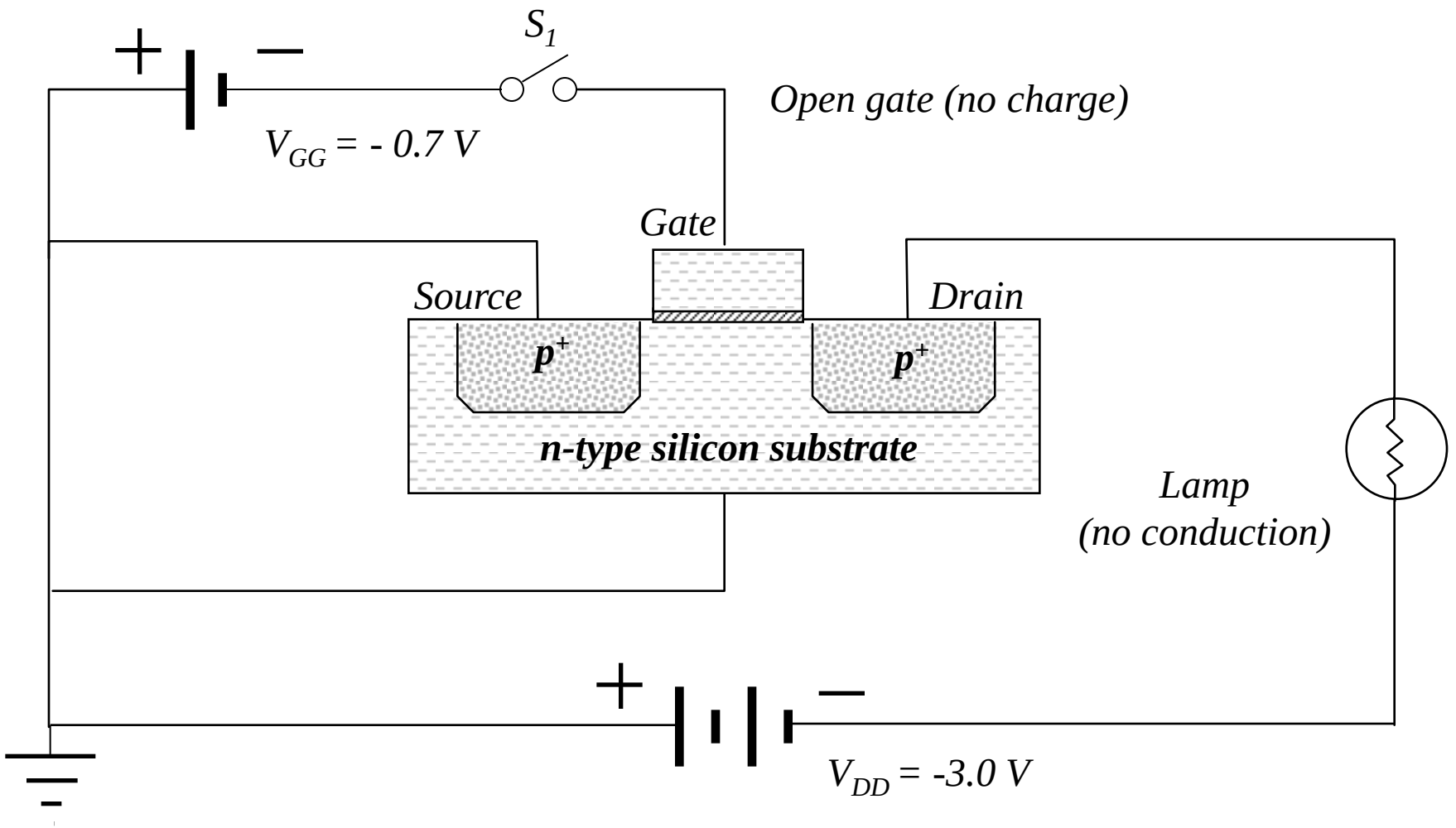


Figure 3.16

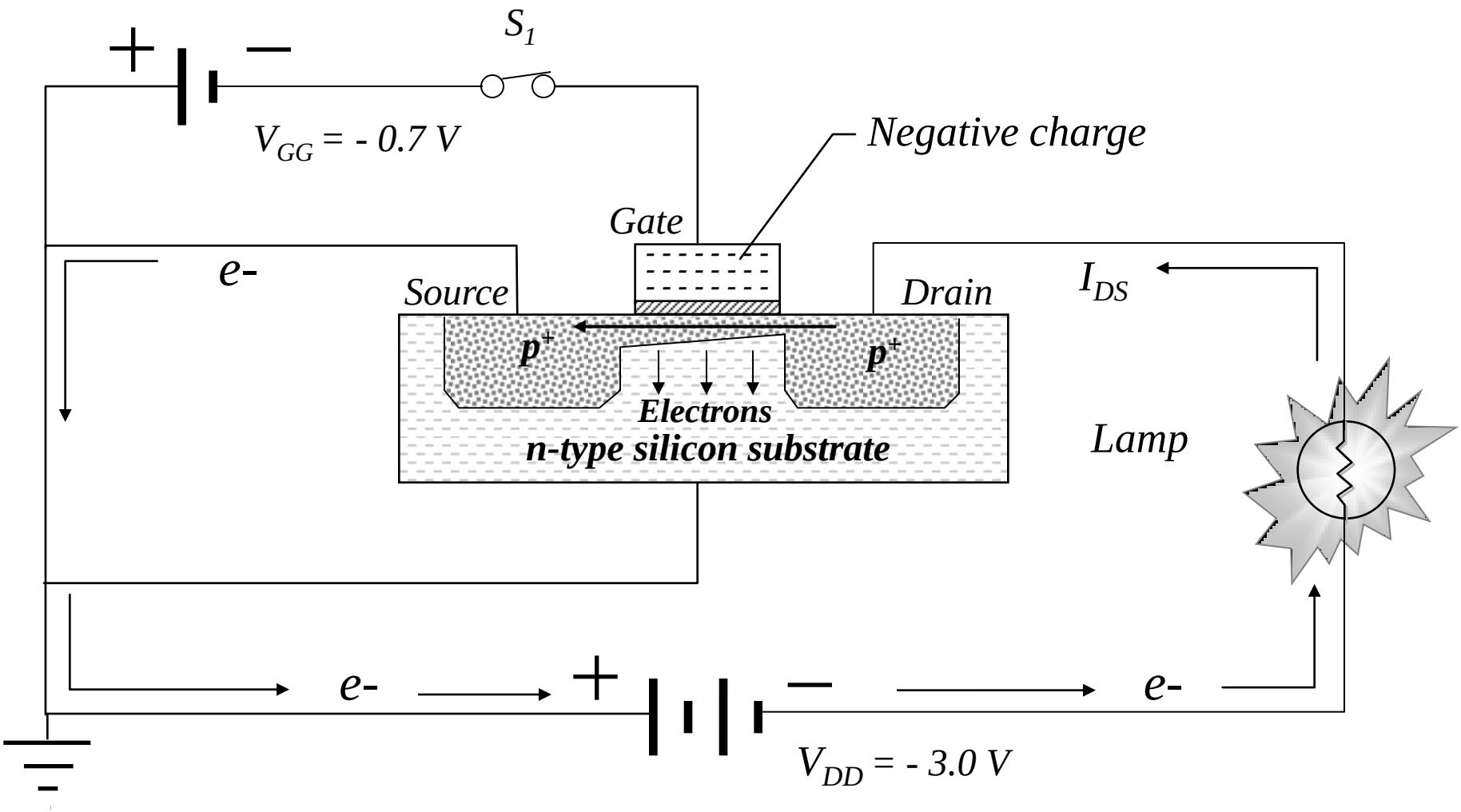
NMOS Transistor in Conduction Mode



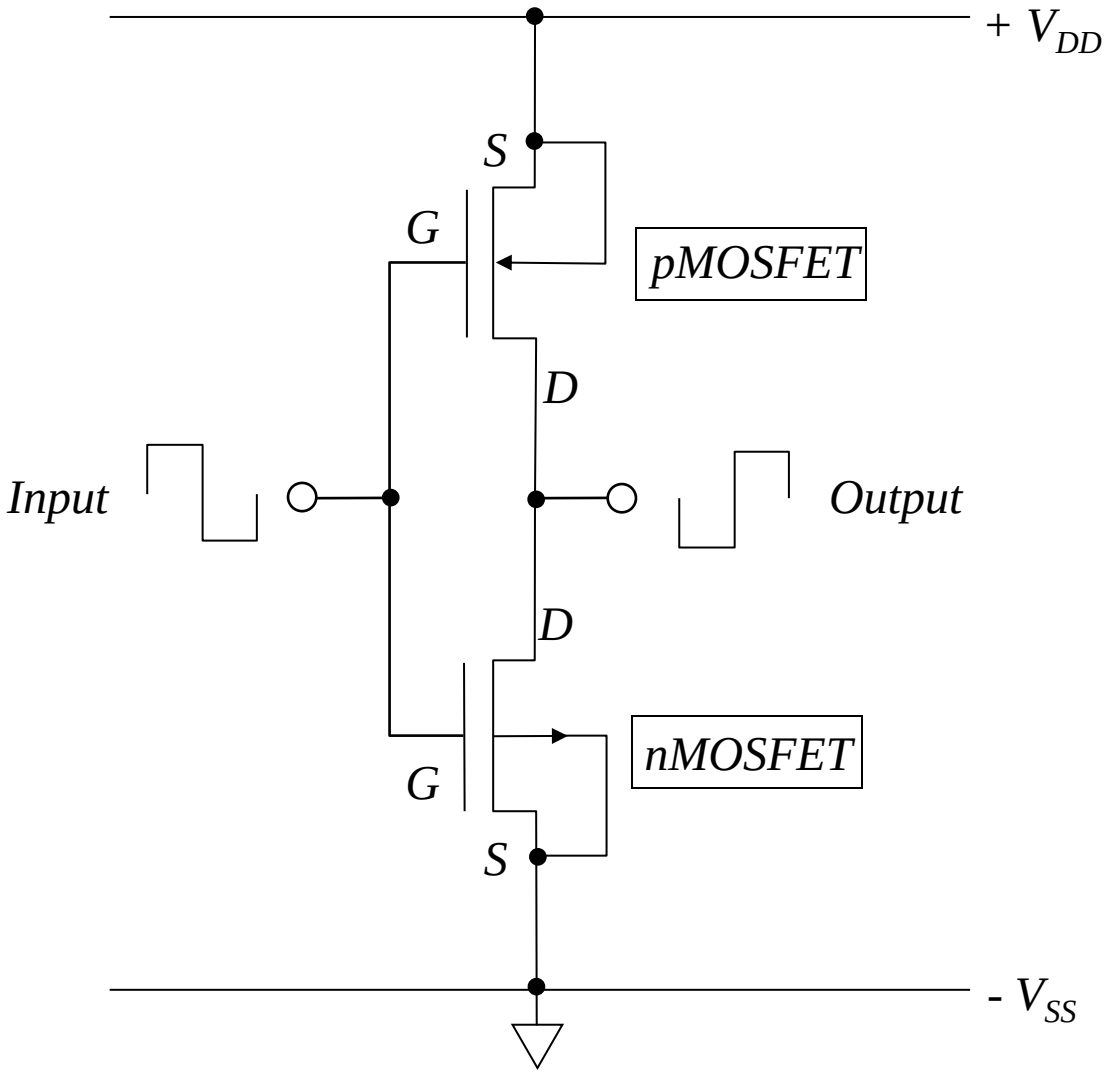
Biasing Circuit for a P-Channel MOSFET



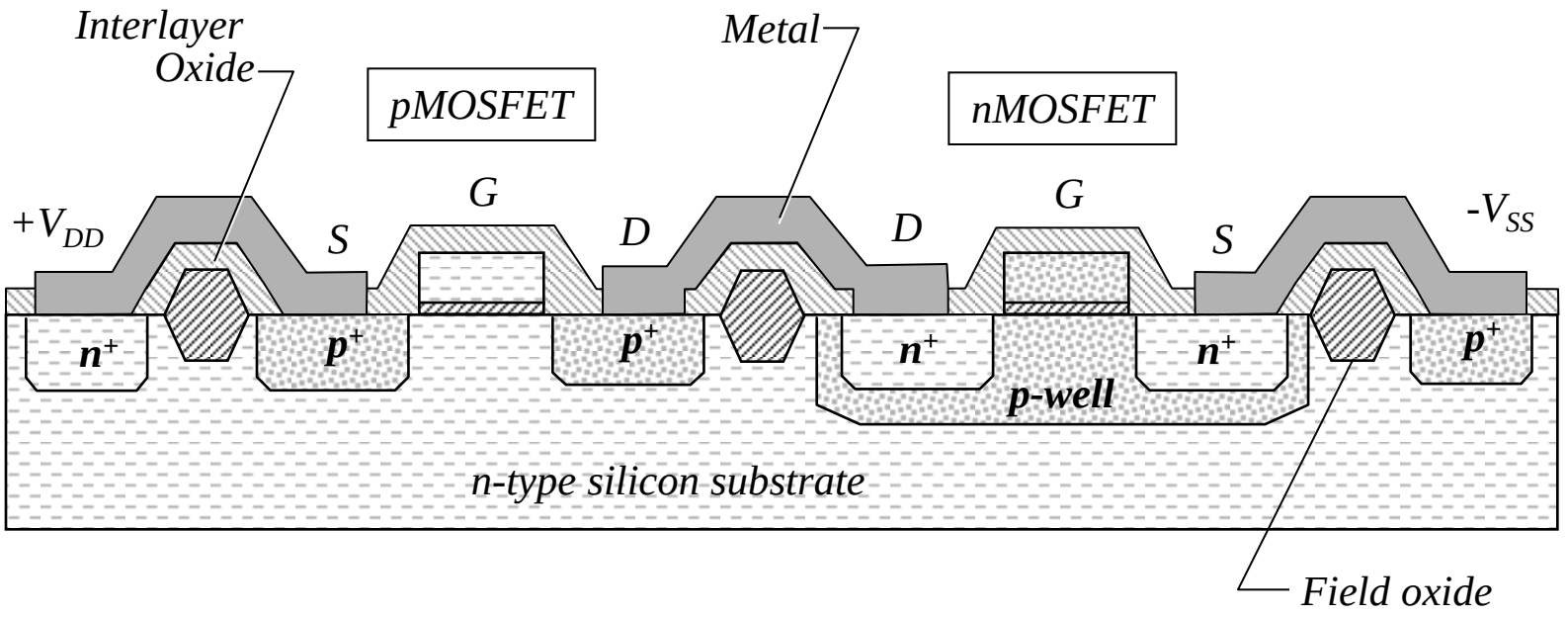
PMOS Transistor in Conduction Mode



Schematic of a CMOS Inverter

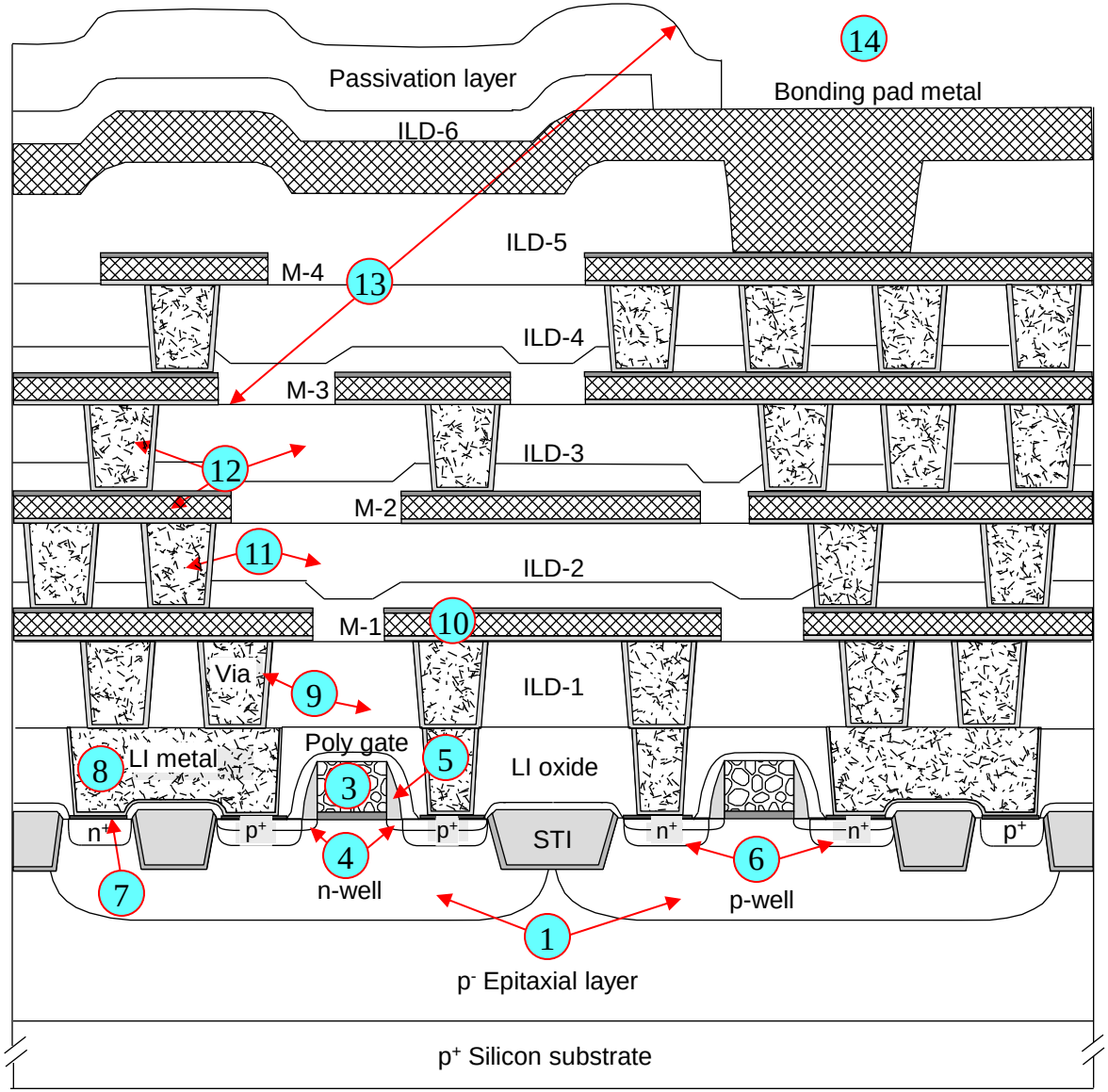


Cross-section of CMOS Inverter



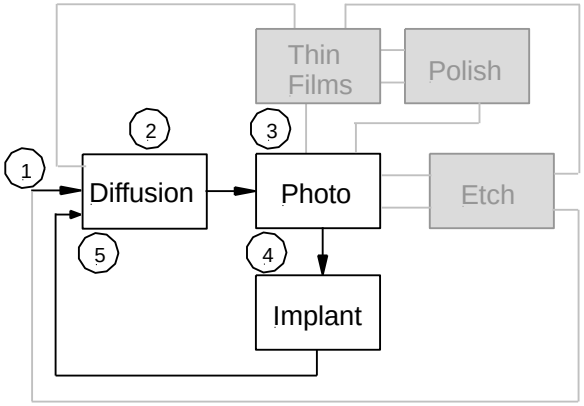
CMOS Manufacturing Steps

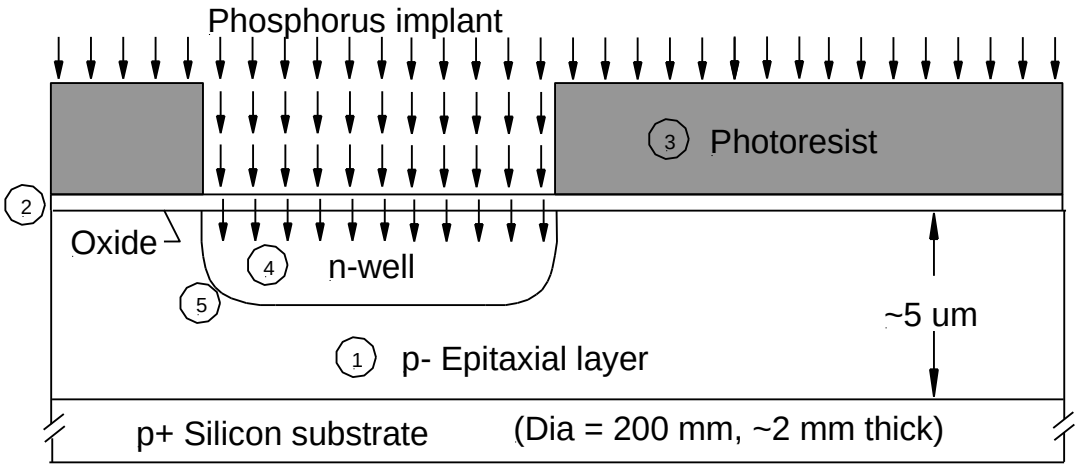
1. Twin-well Implants
2. Shallow Trench Isolation
3. Gate Structure
4. Lightly Doped Drain Implants
5. Sidewall Spacer
6. Source/Drain Implants
7. Contact Formation
8. Local Interconnect
9. Interlayer Dielectric to Via-1
10. First Metal Layer
11. Second ILD to Via-2
12. Second Metal Layer to Via-3
13. Metal-3 to Pad Etch
14. Parametric Testing

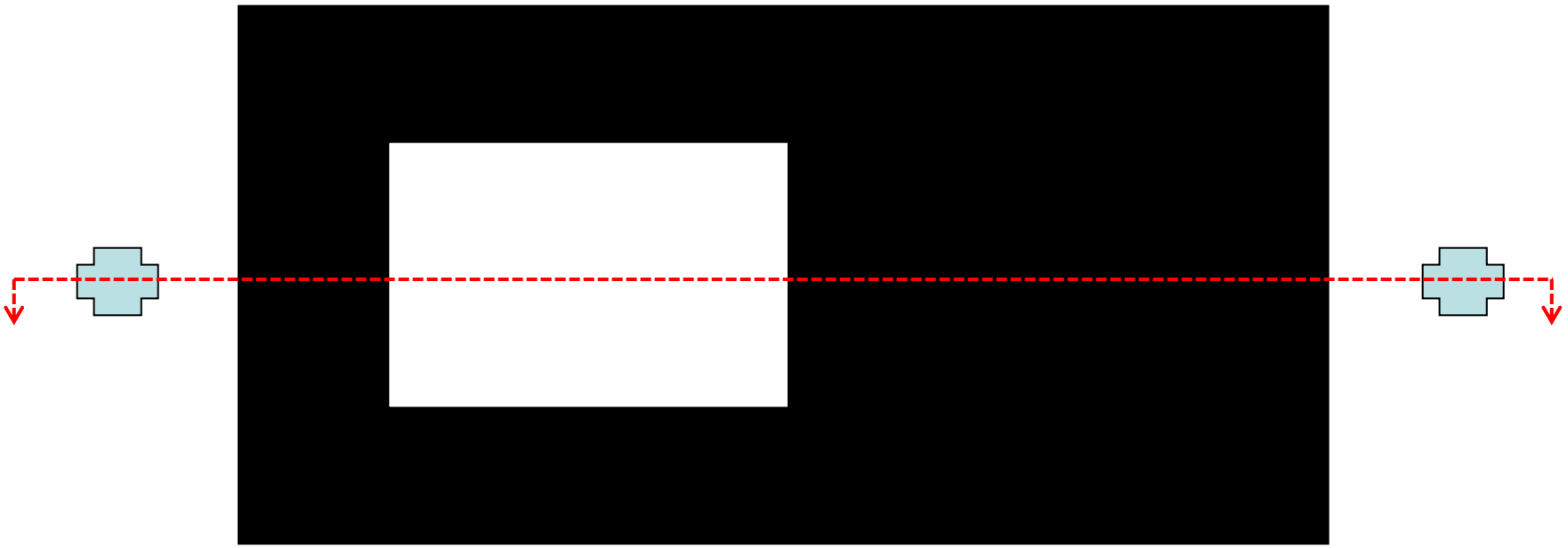


n-well Formation

- Epitaxial layer : improved quality and fewer defect
- In step 2, initial oxide (15 nm) : (1) protects epi layer from contamination, (2) prevents excessive damage to ion/implantation, (3) control the depth of the dopant during implantation
- In step 5, anneal: (1) drive-in, (2) repair damage, (3) activation



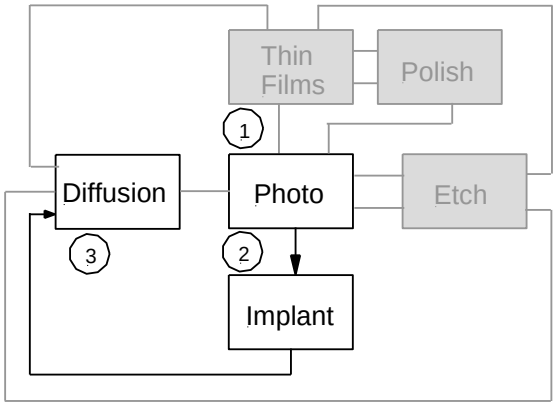


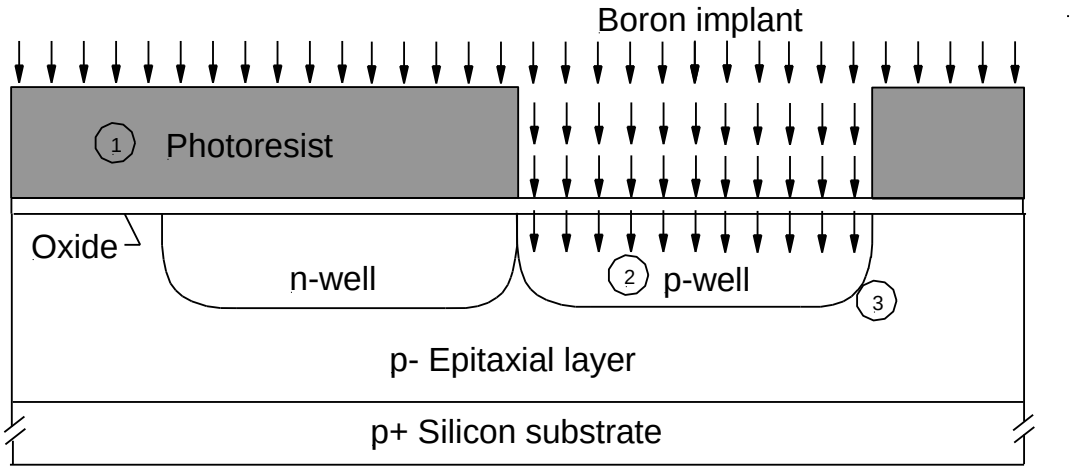


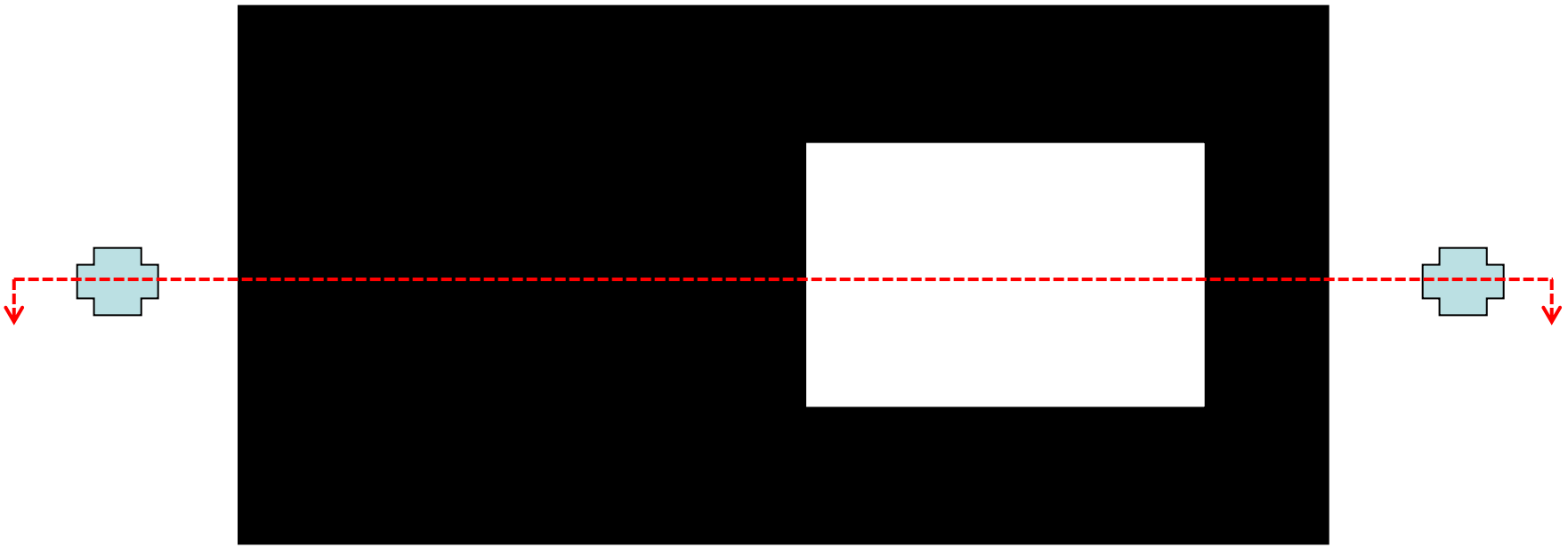
Mask # 1 : N-well formation

p-well Formation

- 2nd mask, this mask is the direct opposite of the n-well implant mask
- Boron is 1/3 the mass of P, so 1/3 energy is used.





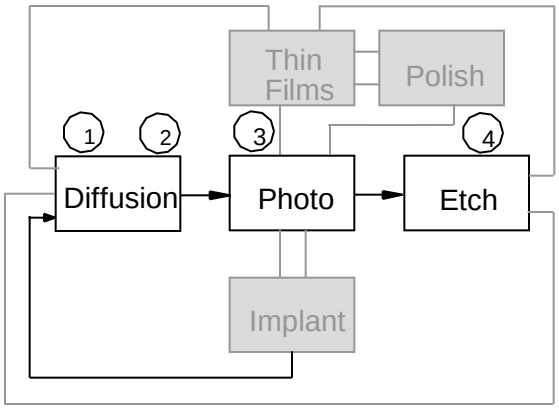


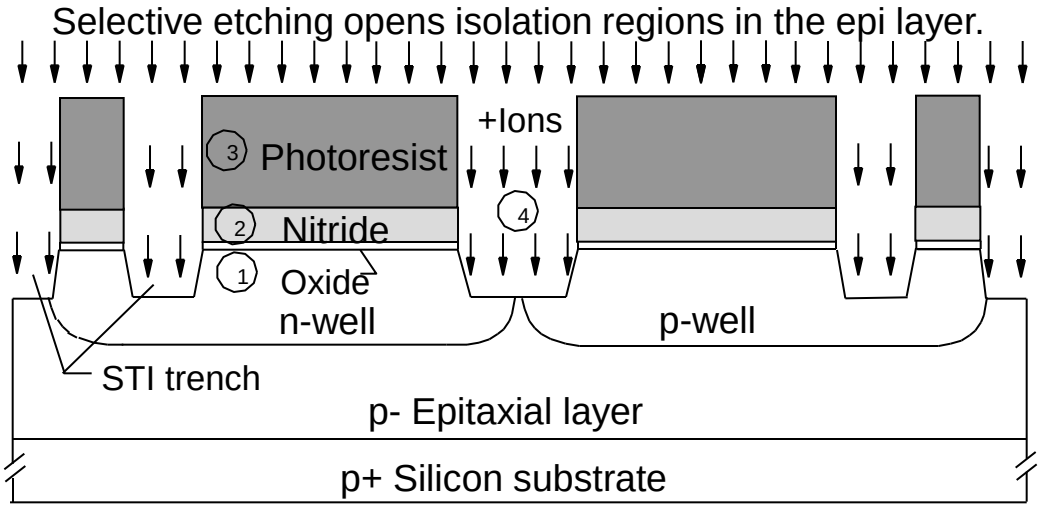
Mask # 2 : P-well formation

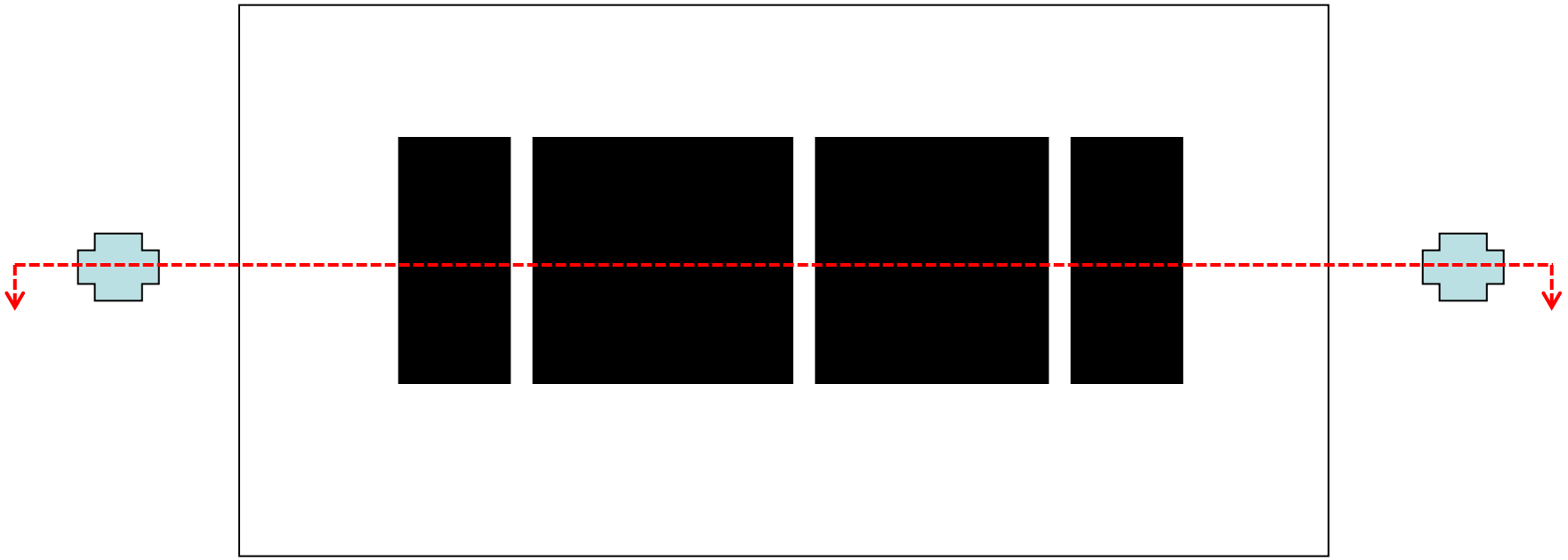
STI Trench Etch

STI: shallow trench isolation

- Barrier oxide: a new oxide
- Nitride: (1) protect active region, (2) stop layer during CMP
- 3rd mask
- STI etching



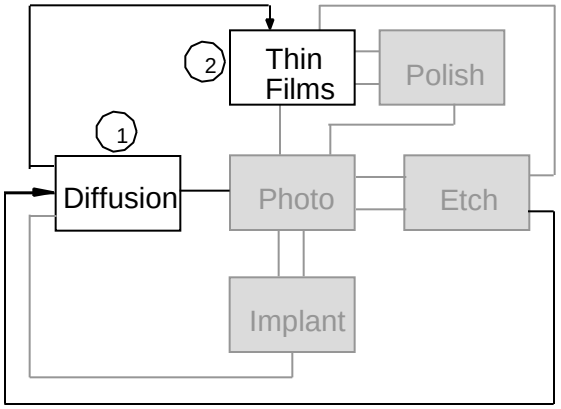


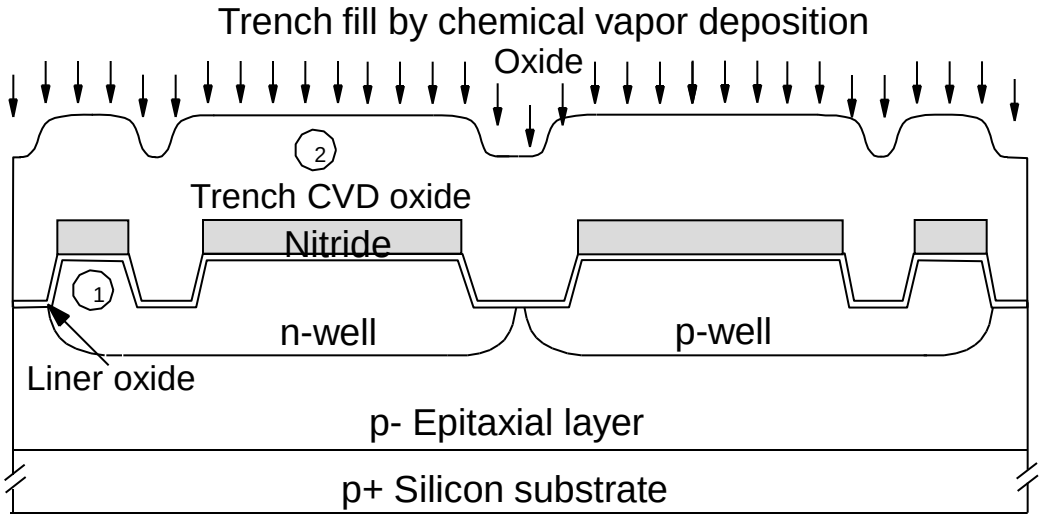


Mask # 3: Shallow Trench Isolation formation

STI Oxide Fill

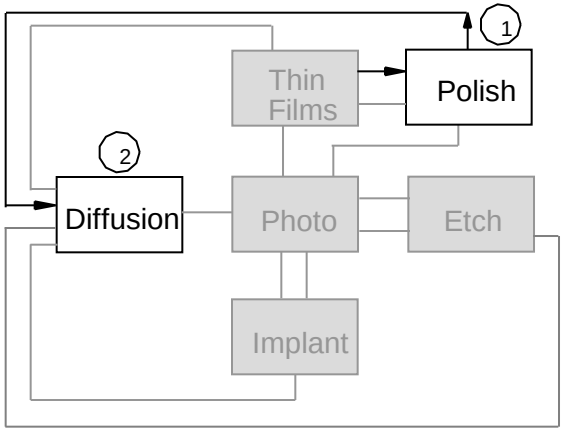
- Liner oxide to improve the interface between the silicon and trench CVD oxide
- CVD oxide deposition or spin-on-glass (SOG)

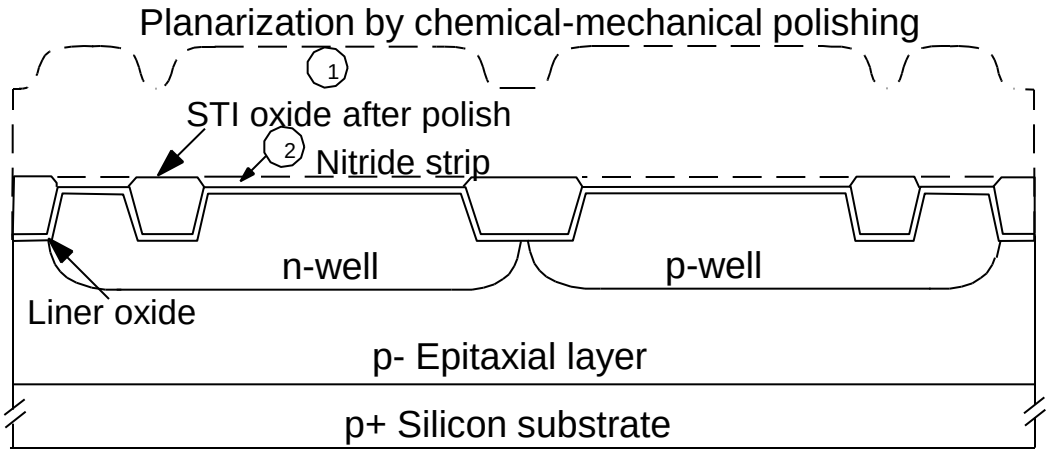




STI Formation

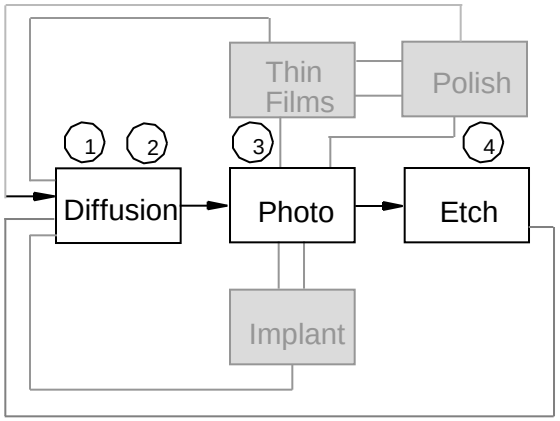
1. Trench oxide polish (CMP): nitride as the CMP stop layer since nitride is harder than oxide
2. Nitride strip: hot phosphoric acid
3. Anti-punch-through and Vth adjustment ion implantation

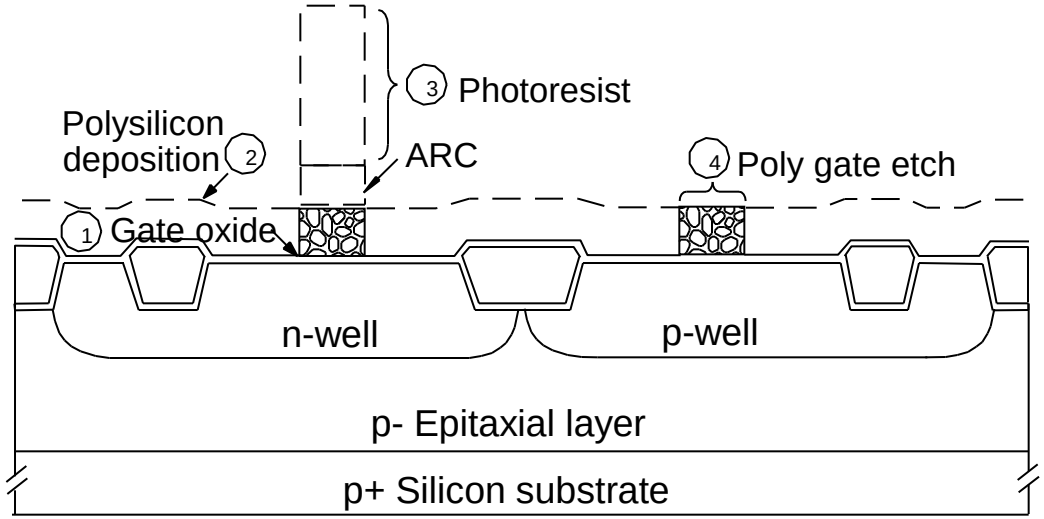


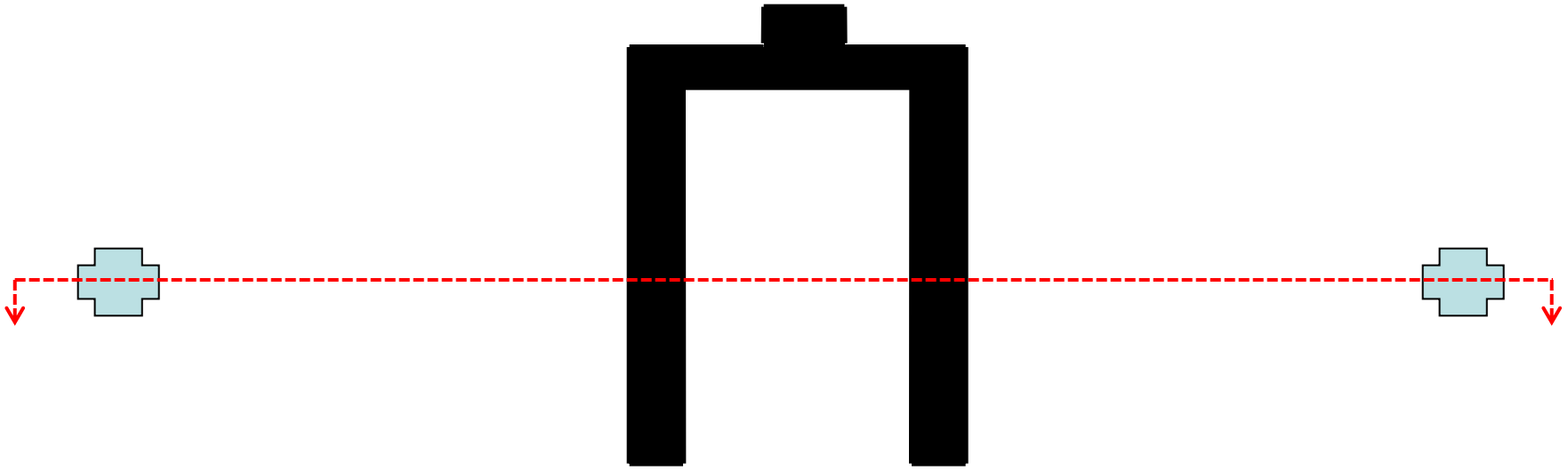


Poly Gate Structure Process

- Oxide thickness 1.5 ~ 5.0 nm is thermal grown
- Poly-Si ~ 300 nm is doped and deposited in LPCVD using SiH_4
- Need Antireflective coating (ARC), very critical
- The most critical etching step in dry etching



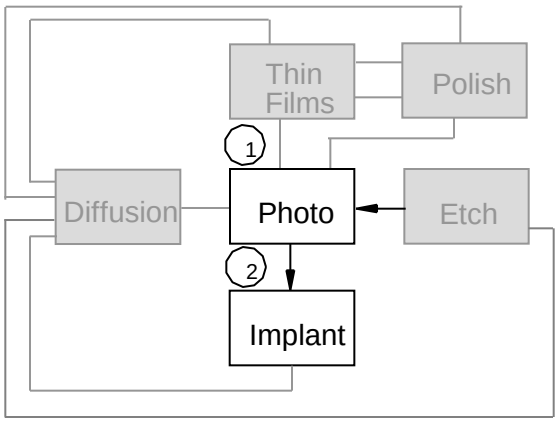


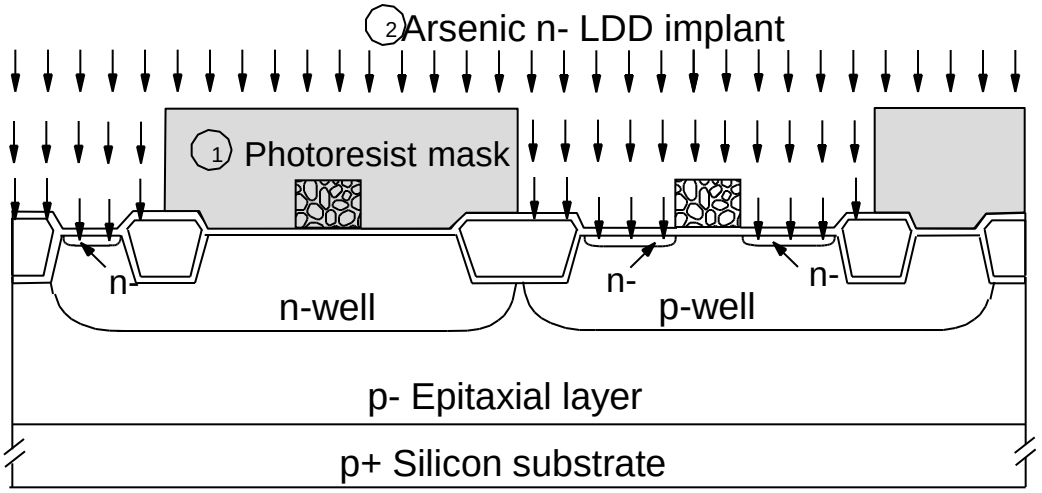


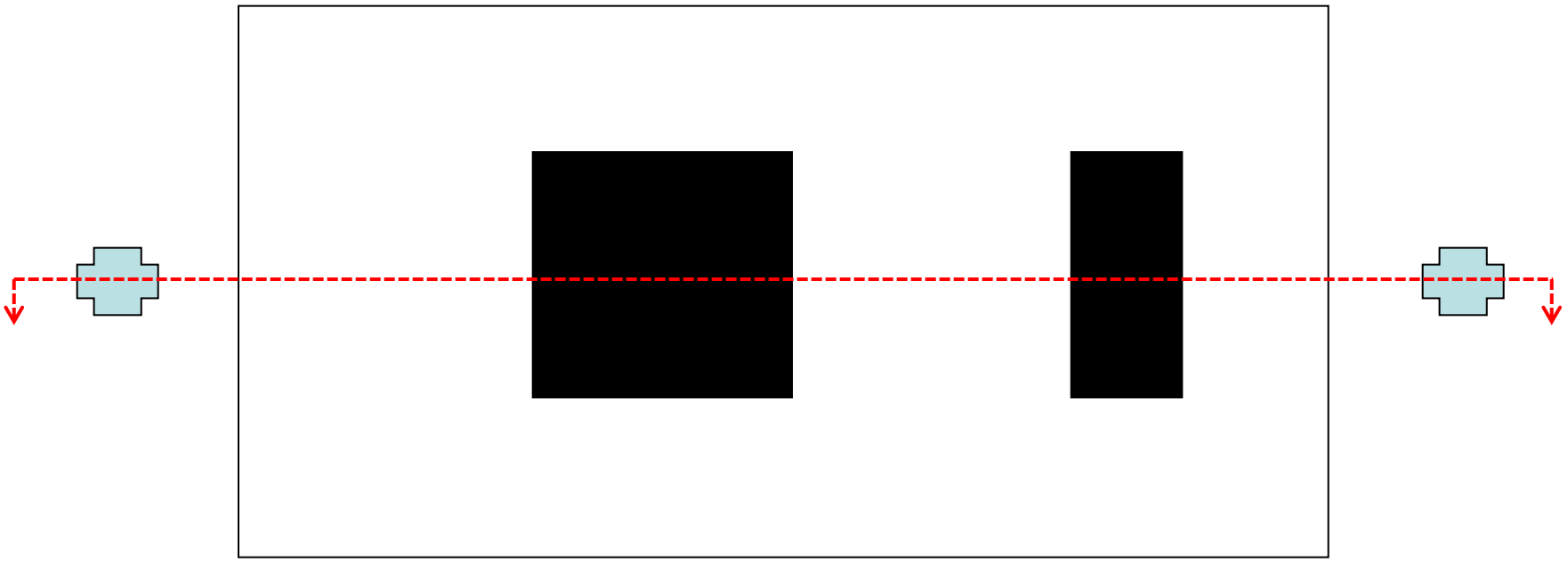
Mask # 4 :Poly-Si gate formation

n^- LDD Implant

- LDD: lightly doped drain to reduce S/D leakage
- Large mass implant (BF_2, instead of B, As instead of P) and amorphous surface helps maintain a shallow junction
- 5^{th} mask



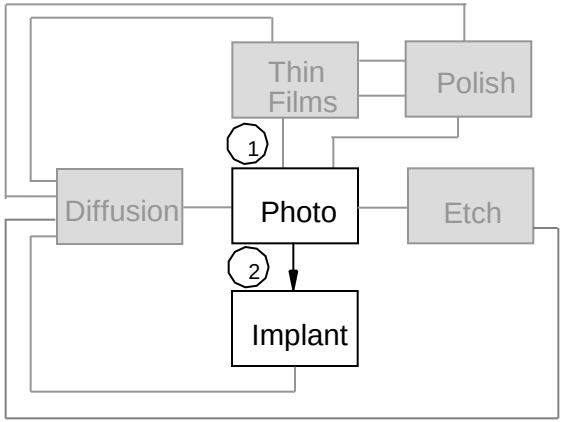


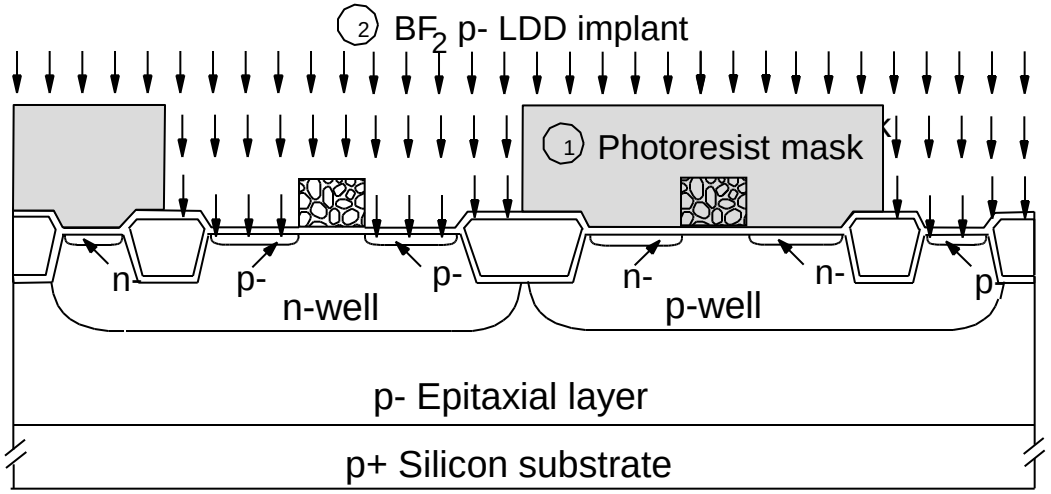


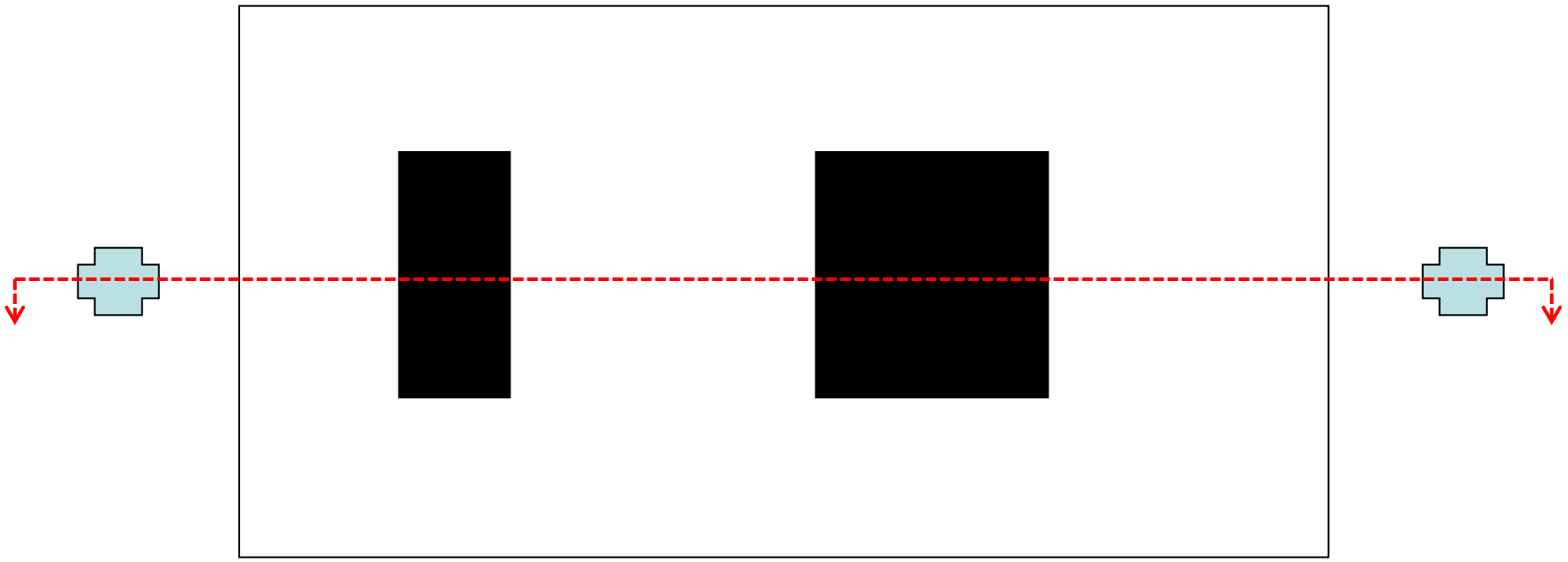
Mask # 5: N^- LDD formation

p^- LDD Implant

- 6th mask
- In modern device, high doped drain is used to reduce series resistance. It called S/D extension



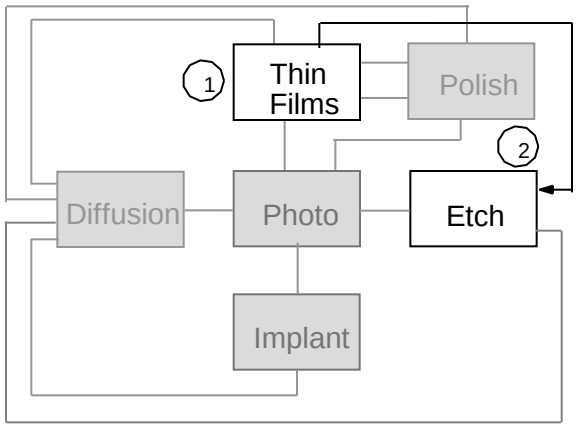


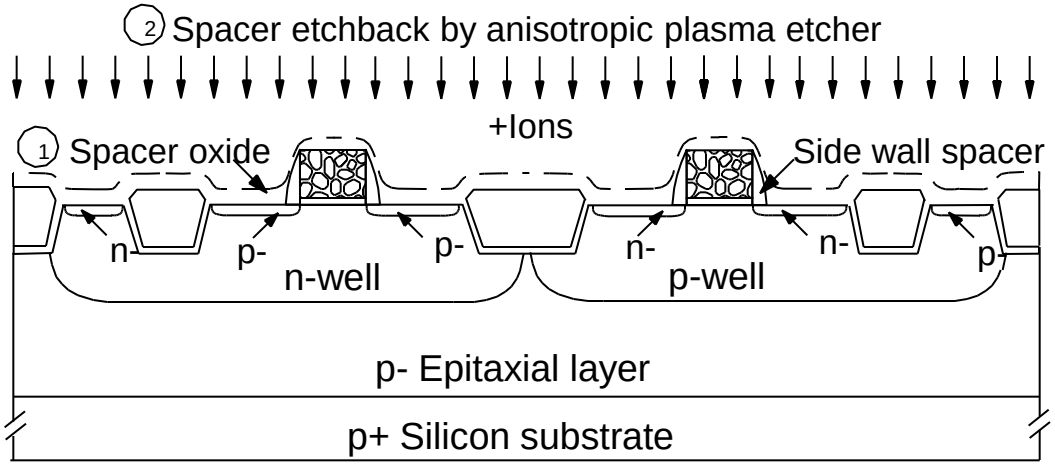


Mask # 6: P^- LDD formation

Side Wall Spacer Formation

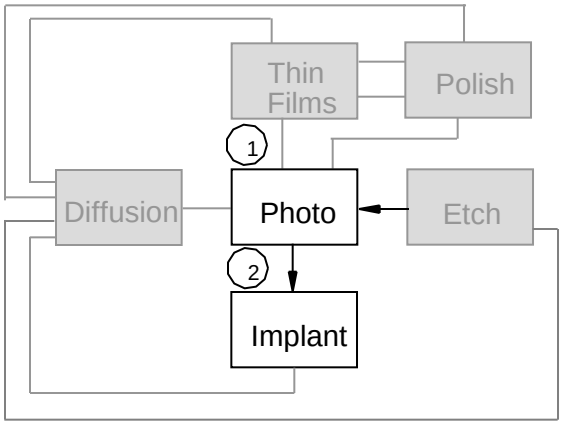
- Spacer is used to prevent higher S/D implant from penetrating too close to the channel, cover LDD.
- CVD oxide + etch back by anisotropic plasma etching

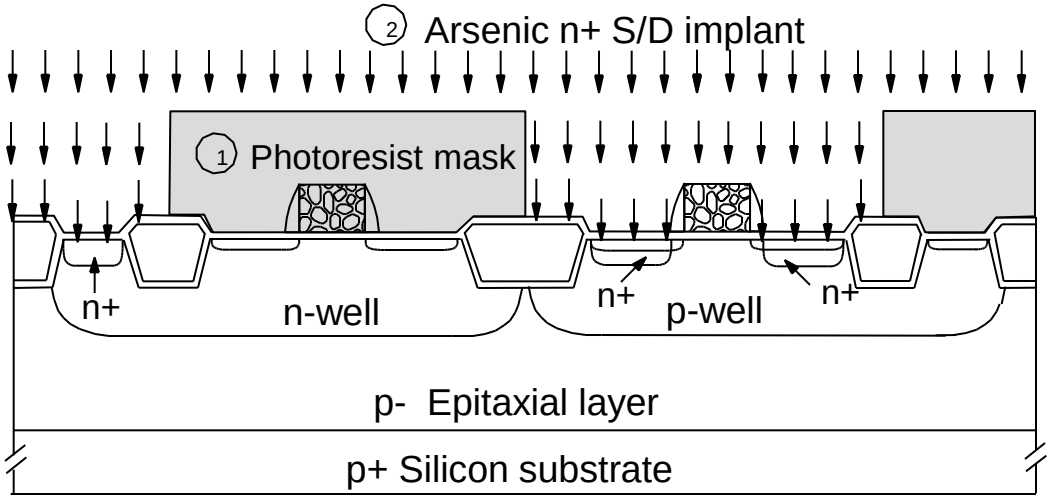


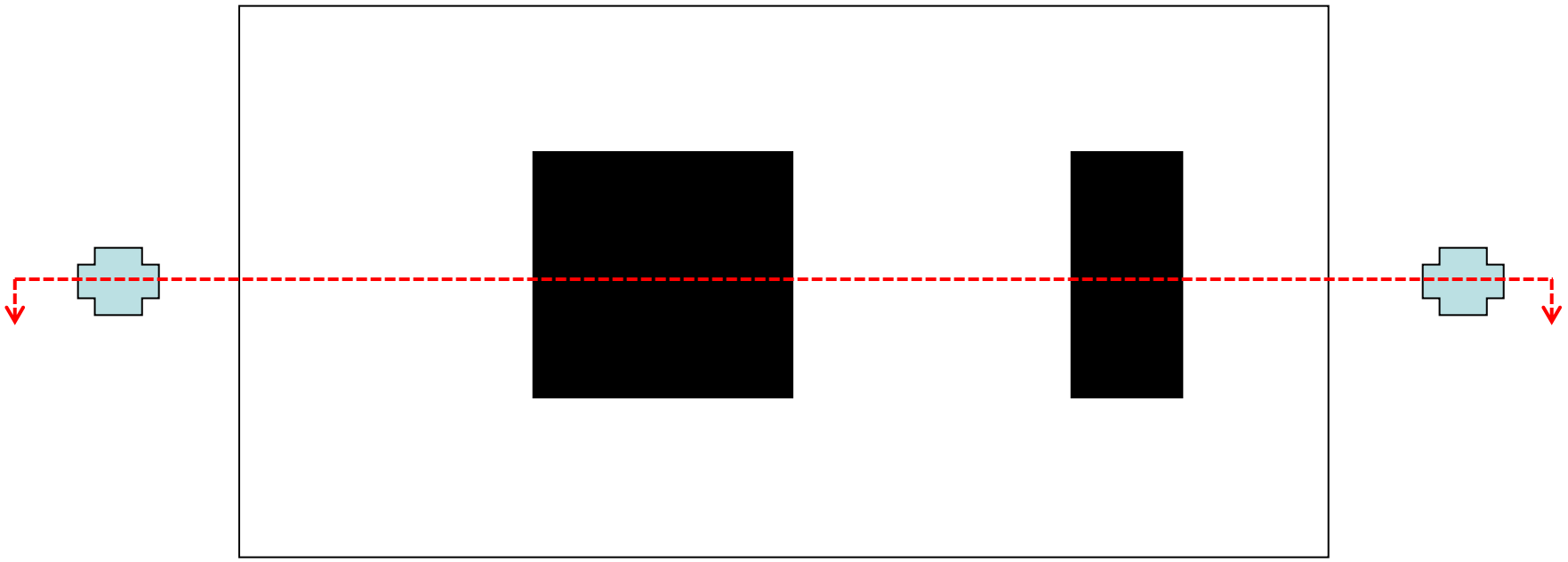


n^+ Source/Drain Implant

- Energy is high than LDD I/I, the junction is deep
- 7^{th} mask



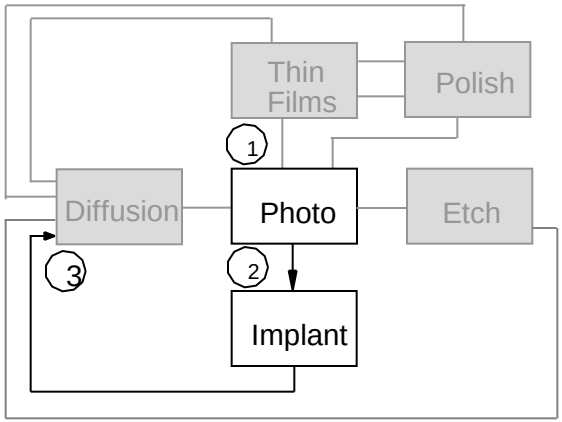


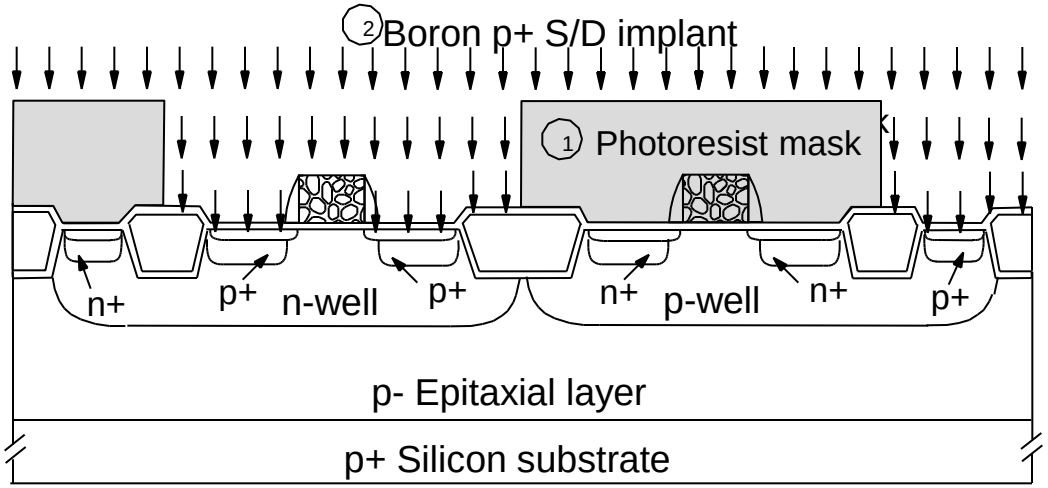


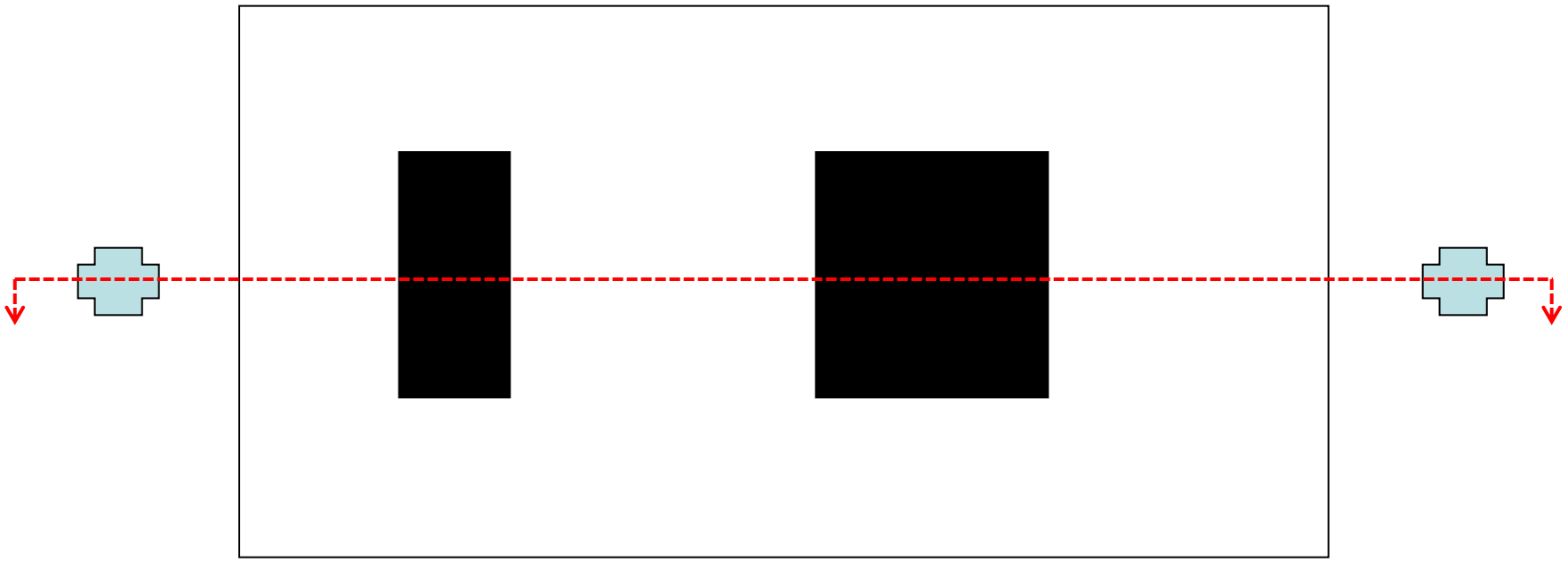
Mask # 7: N^+ Source/Drain formation

p^+ Source/Drain Implant

- 8th mask
- Using rapid thermal anneal (RTA) to prevent dopant spreading and to control diffusion of dopant



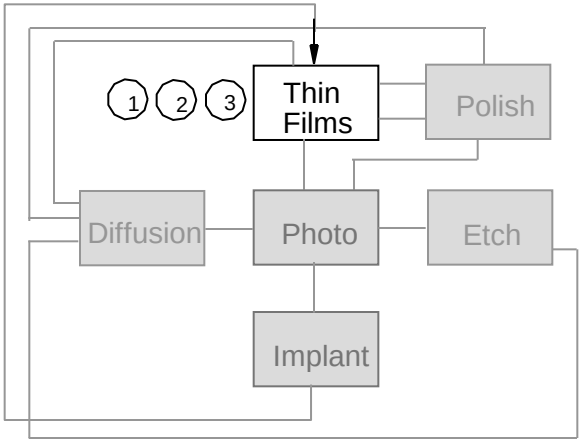


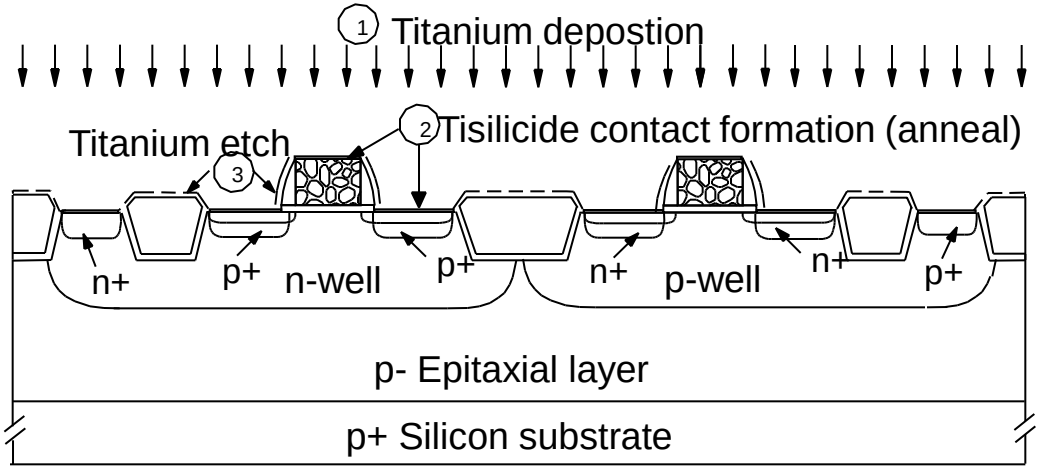


Mask # 8 : P^+ Source/Drain formation

Contact Formation

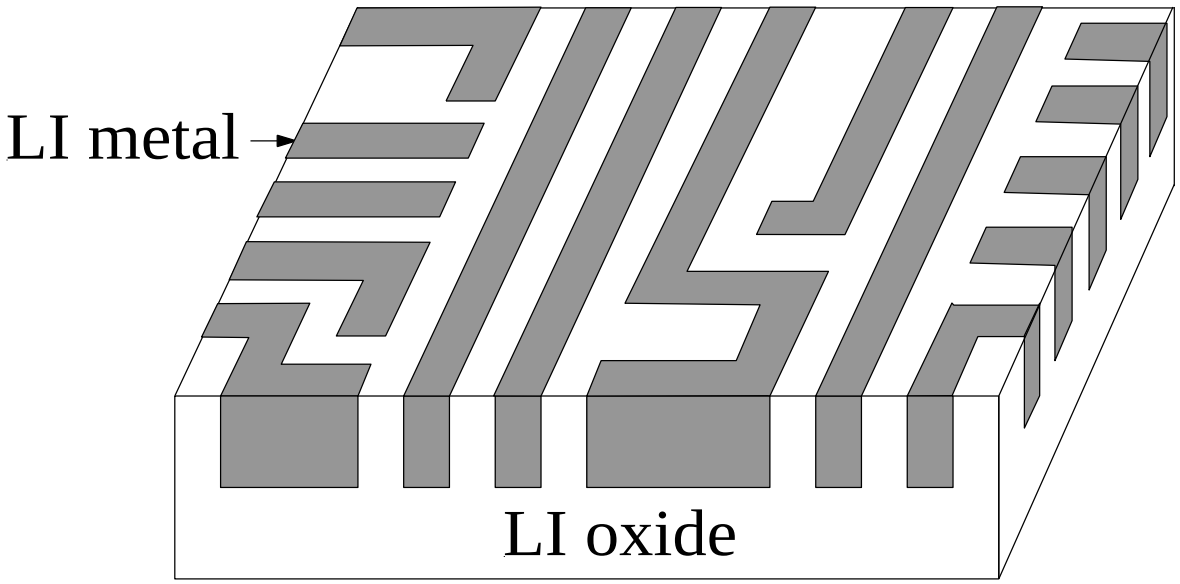
- Titanium (Ti) is a good choice for metal contact due to low resistivity and good adhesion
- No mask needed, called self-align
- Using Ar to sputtering metal
- Anneal to form $TiSi_2$, tisilicide
- Chemical etching to remove unreact Ti, leaving $TiSi_2$, called selective etching





LI Oxide as a Dielectric for Inlaid LI Metal (Damascene)

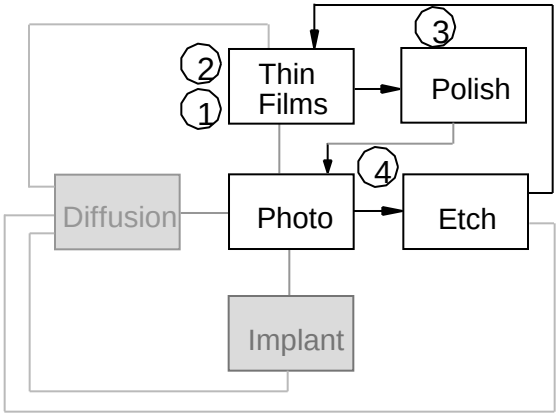
- Damascene: a name doped of year ago from a practice that began thousands ago by artist in Damascus, Syria

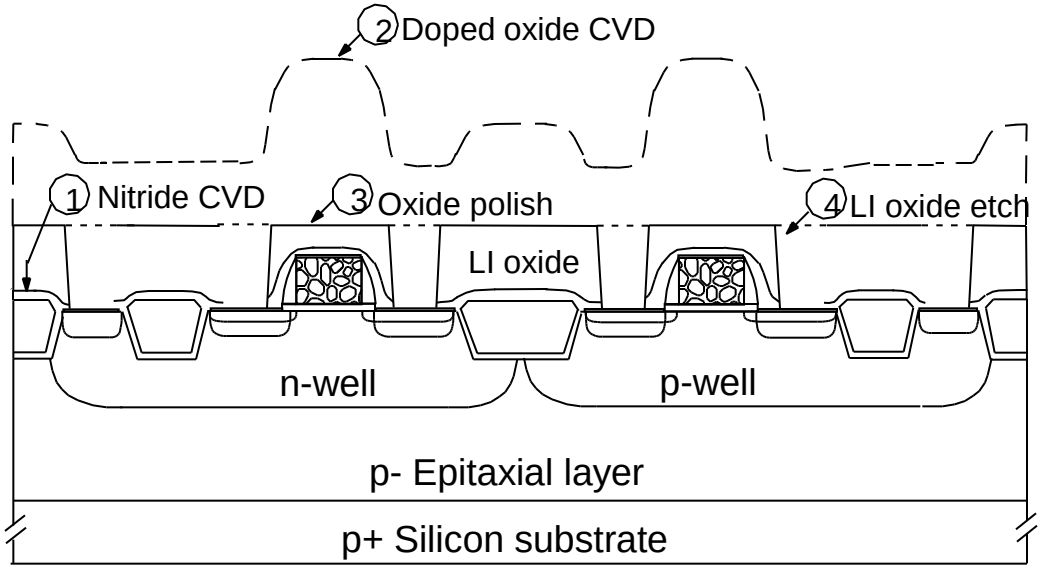


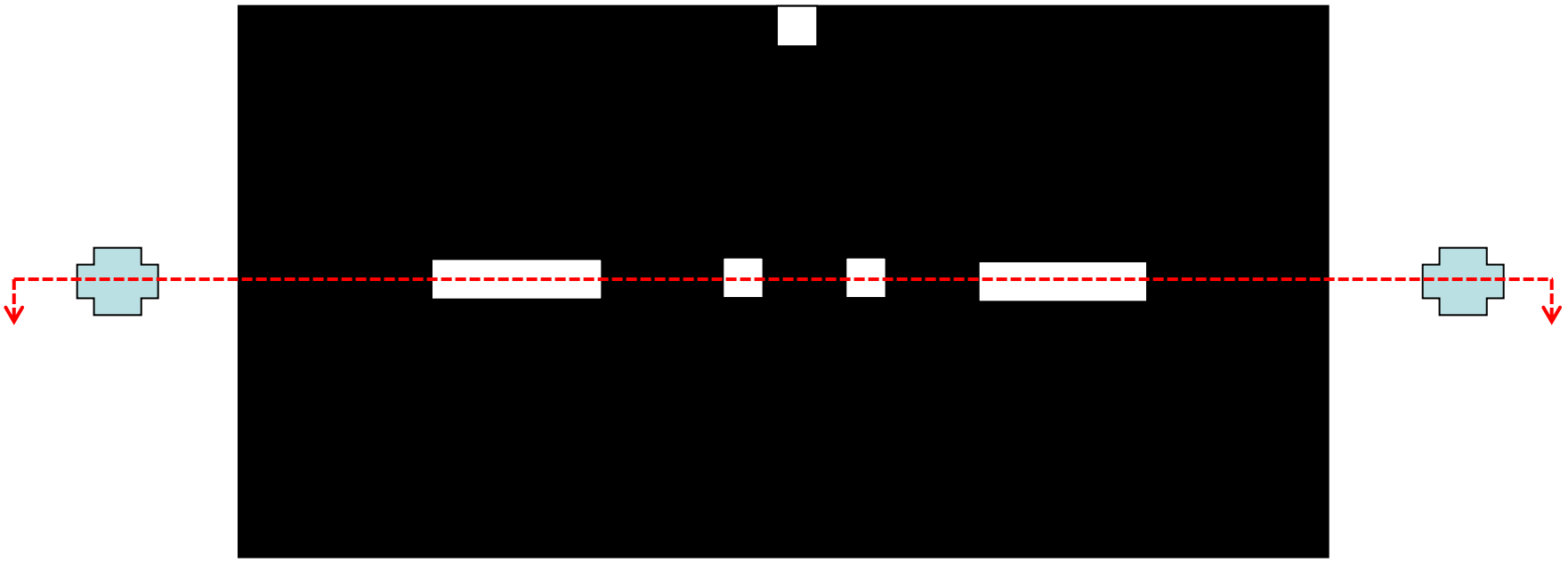
LI: local interconnection

LI Oxide Dielectric Formation

- Nitride: protect active region
- Doped oxide
- Oxide polish
- 9th mask



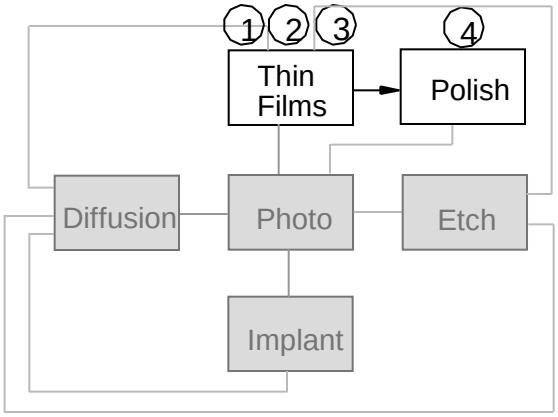


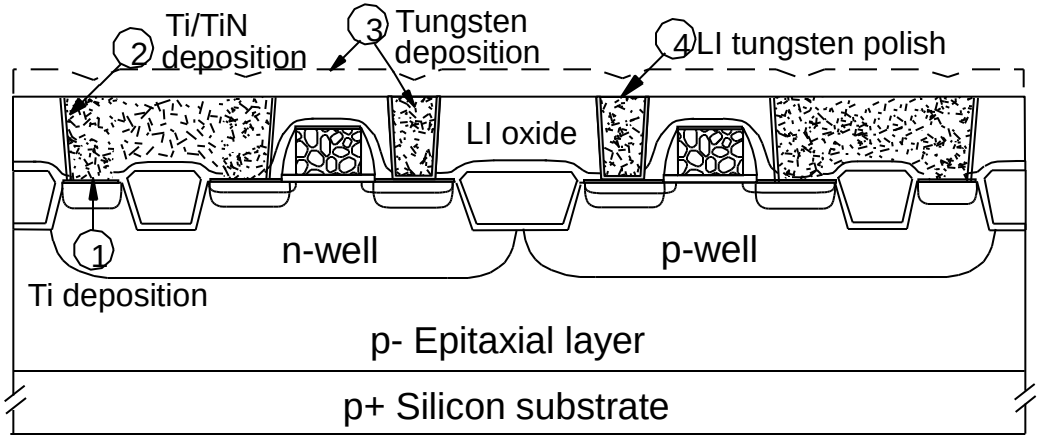


Mask # 9: Local Interconnection formation

LI Metal Formation

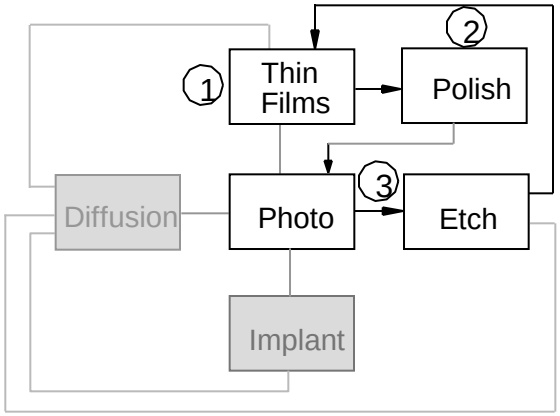
- Ti/TiN is used: Ti for adhesion and TiN for diffusion barrier
- Tungsten (W) is preferred over Aluminum (Al) for LI metal due to its ability to fill holes without leaving voids

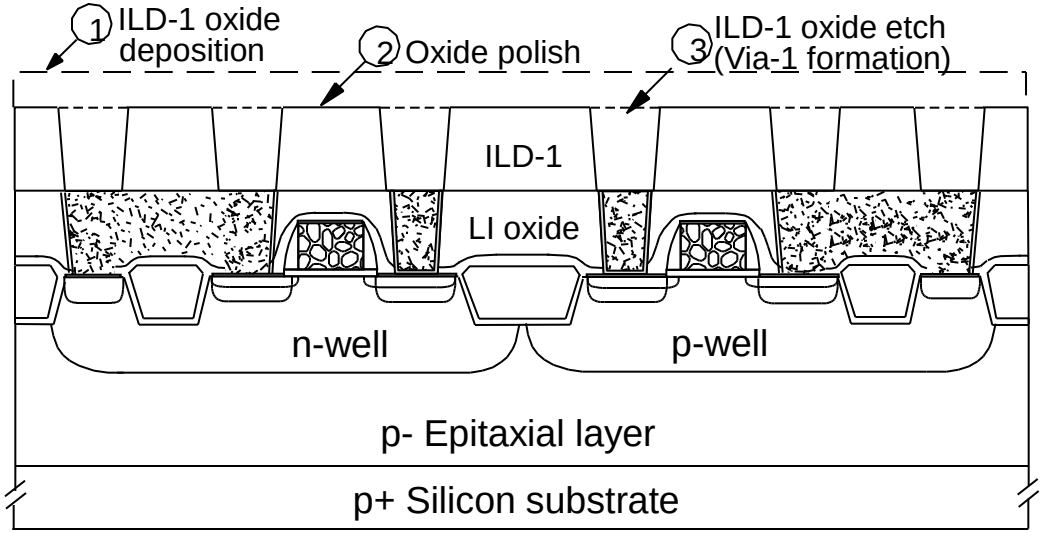


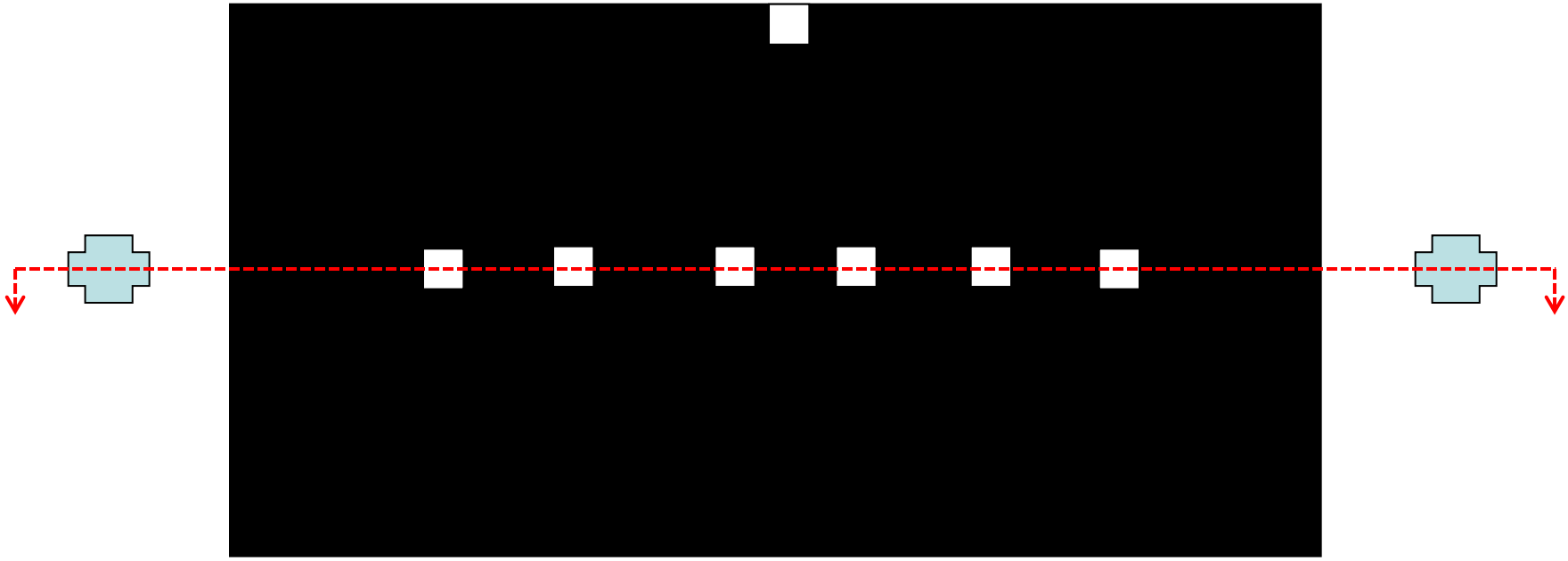


Via-1 Formation

- Interlayer dielectric (ILD): insulator between metal (800nm)
- Via: electrical pathway from one metal layer to adjacent metal layer
- 10th mask



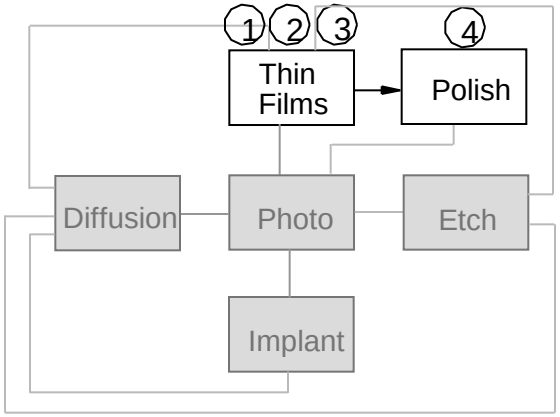


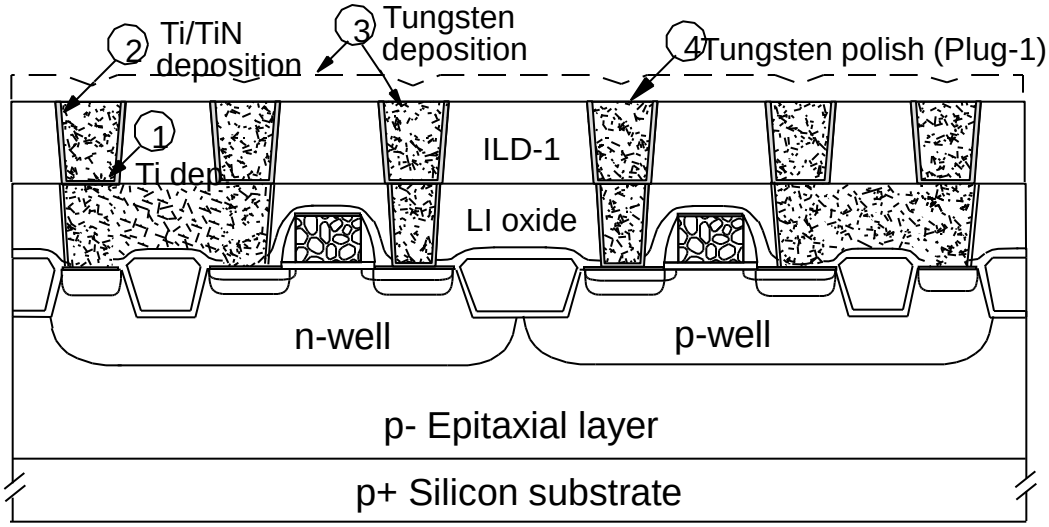


Mask # 10: Via-1 formation

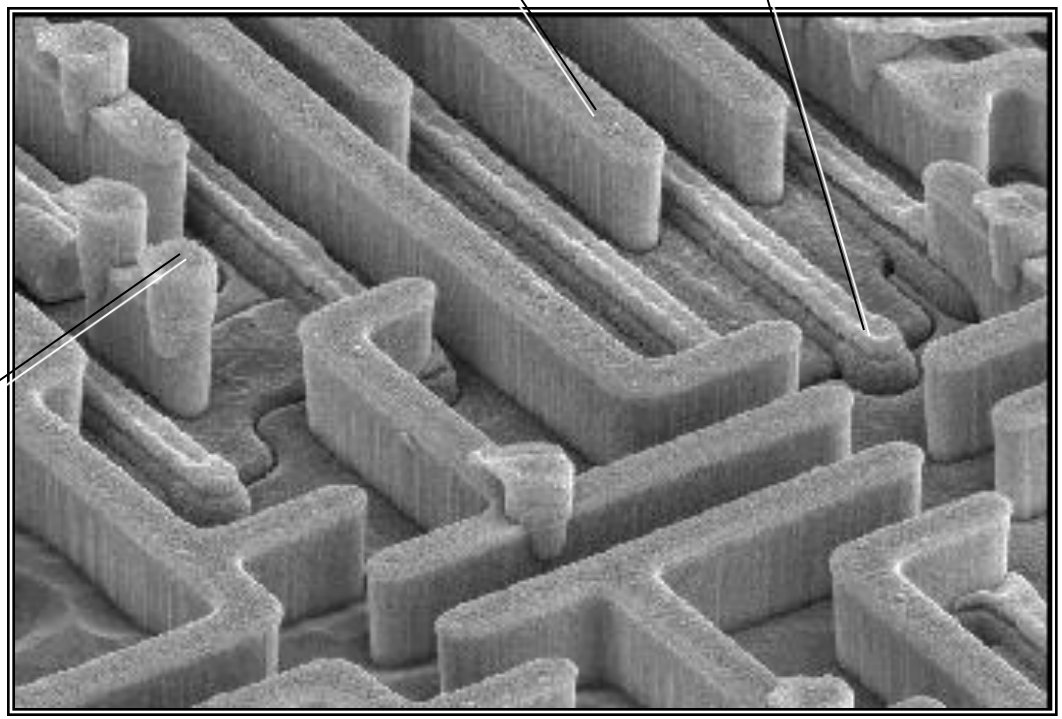
Plug-1 Formation

- Ti layer as a glue layer to hold W
- TiN layer as the diffusion barrier
- Tungsten (W) as the via
- CMP W-polish





SEM Micrographs of Polysilicon, Tungsten LI and Tungsten Plugs

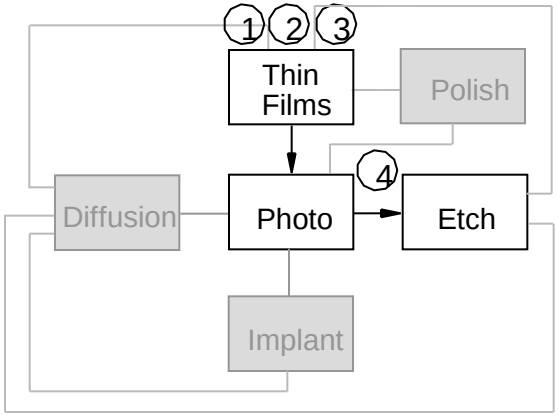


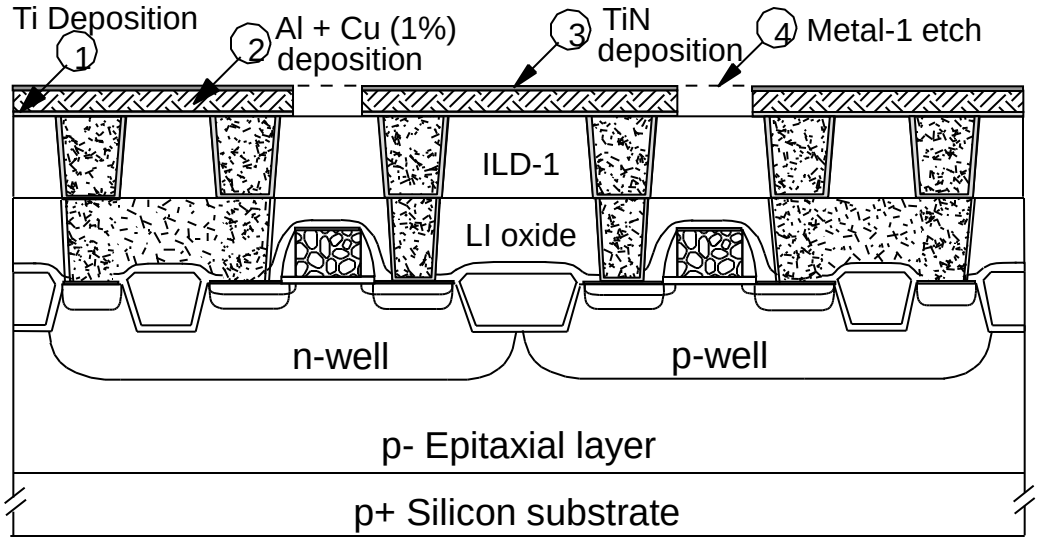
Mag. 17,000 X

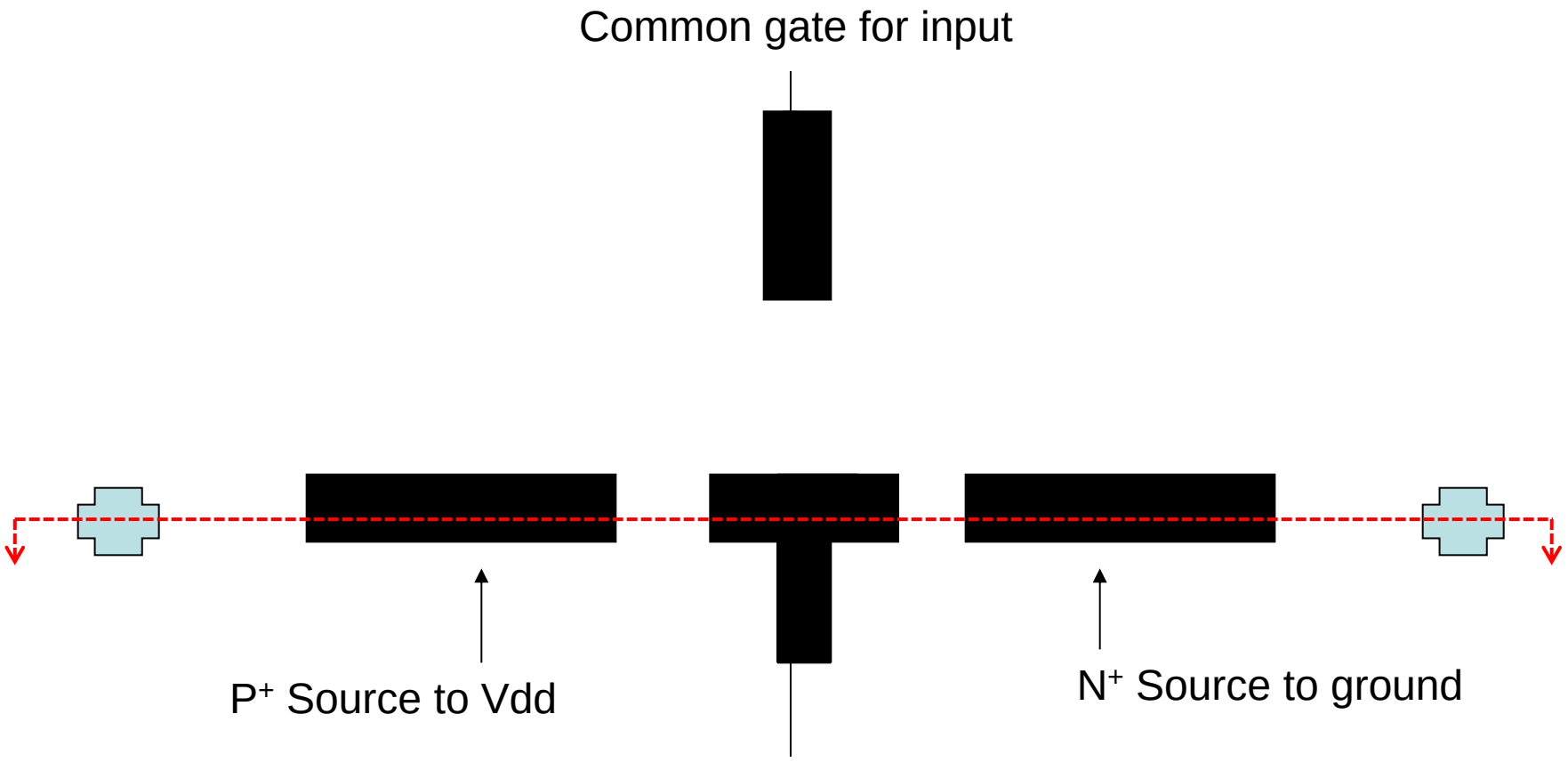
Micrograph courtesy of Integrated Circuit Engineering

Metal-1 Interconnect Formation

- Metal stack: Ti/Al (or Cu)/TiN is used
- Al(99%) + Cu (1%) is used to improve reliability
- 11th mask

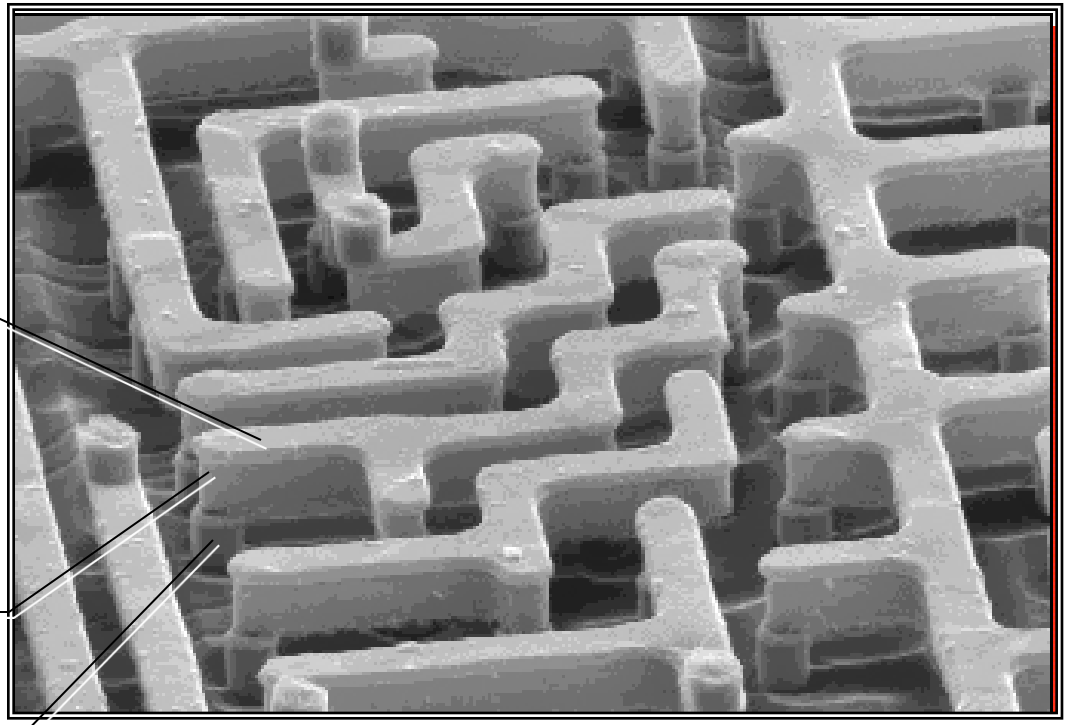






Mask # 11: Metal-1 formation

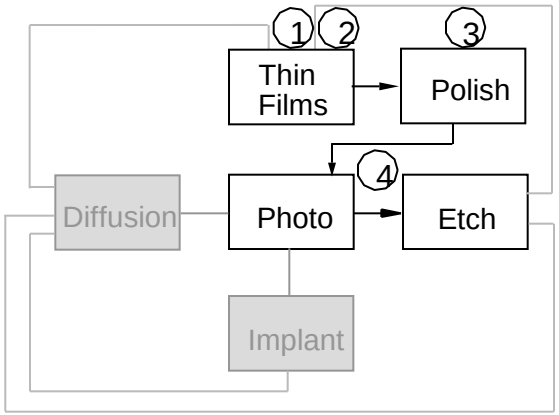
SEM Micrographs of First Metal Layer over First Set of Tungsten Vias

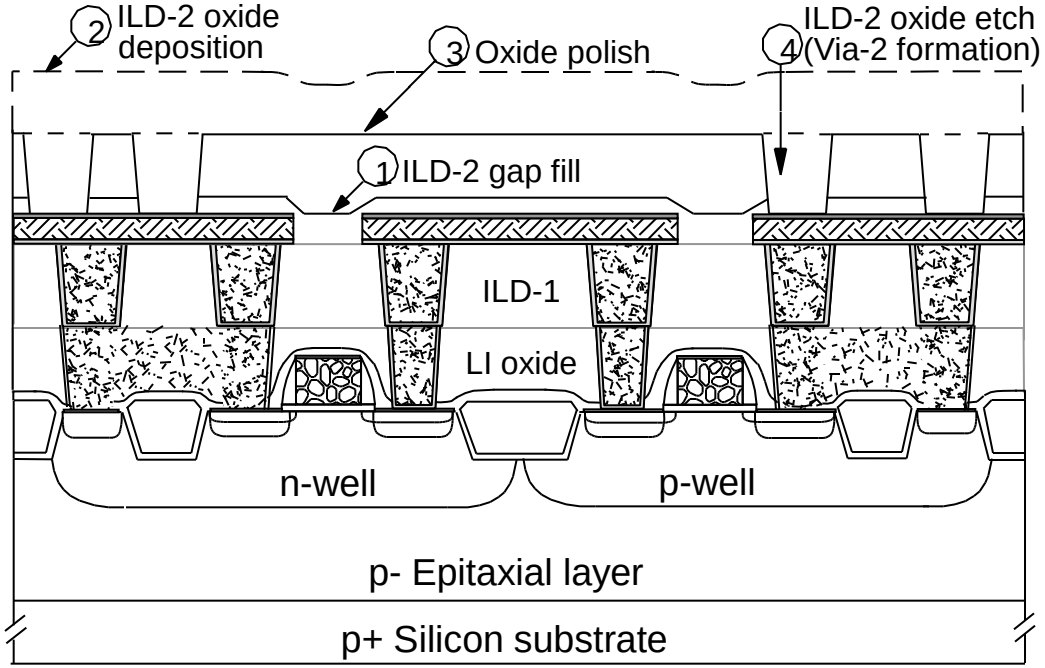


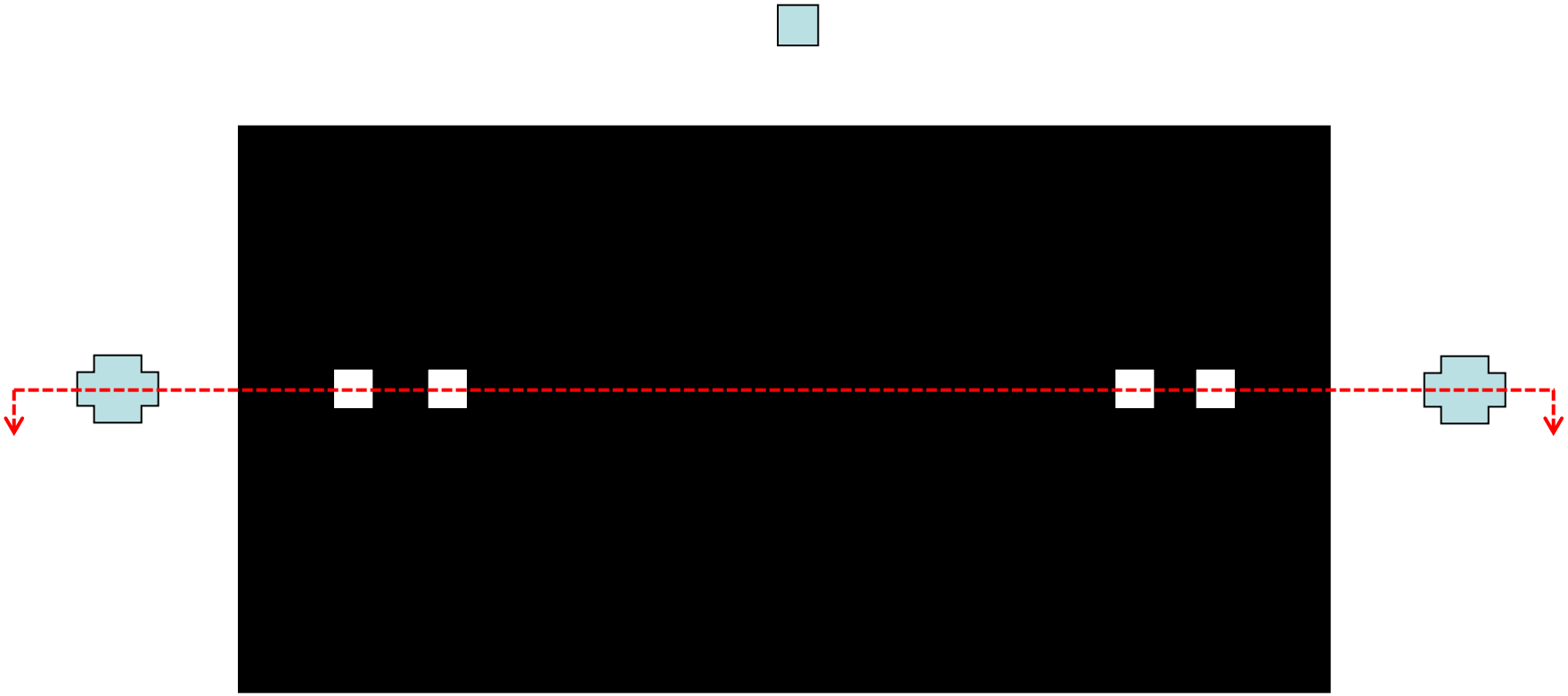
Micrograph courtesy of Integrated Circuit Engineering

Via-2 Formation

- Gap fill: fill the gap between metal
- Oxide deposition
- Oxide polish
- 12th mask



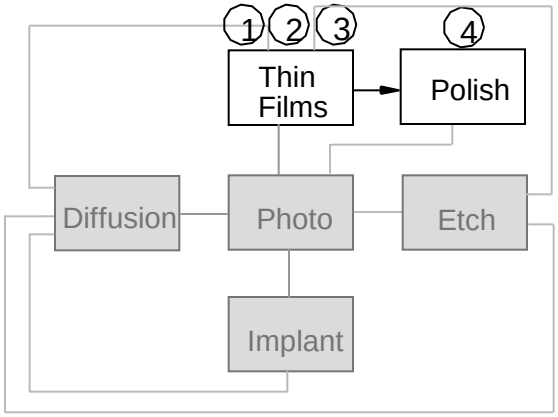


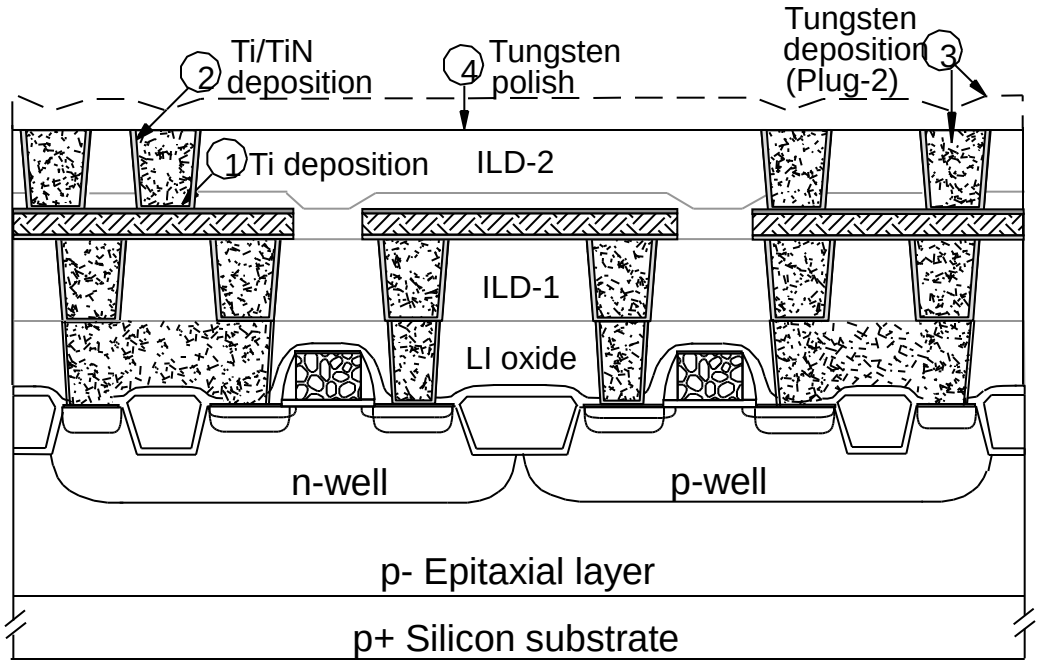


Mask # 12: Via-2 formation

Plug-2 Formation

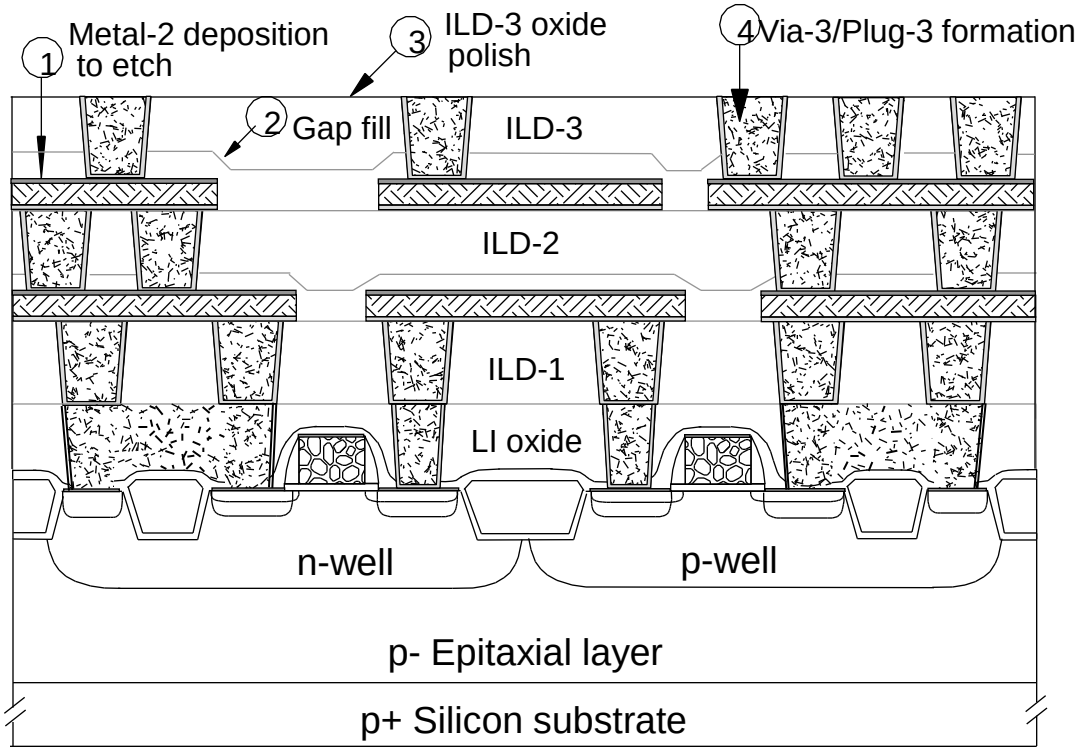
- Ti/TiN/W
- CMP W polish

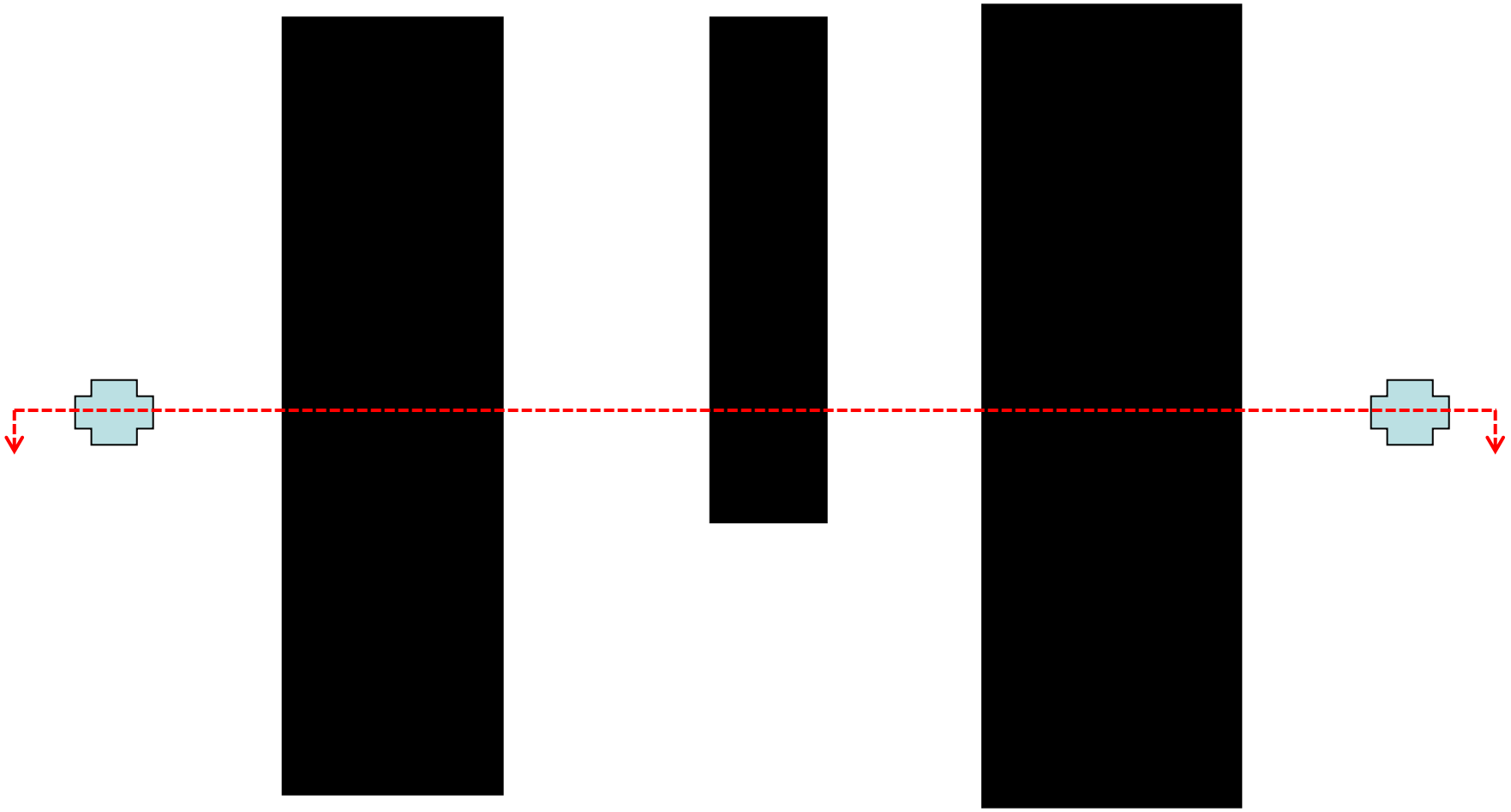




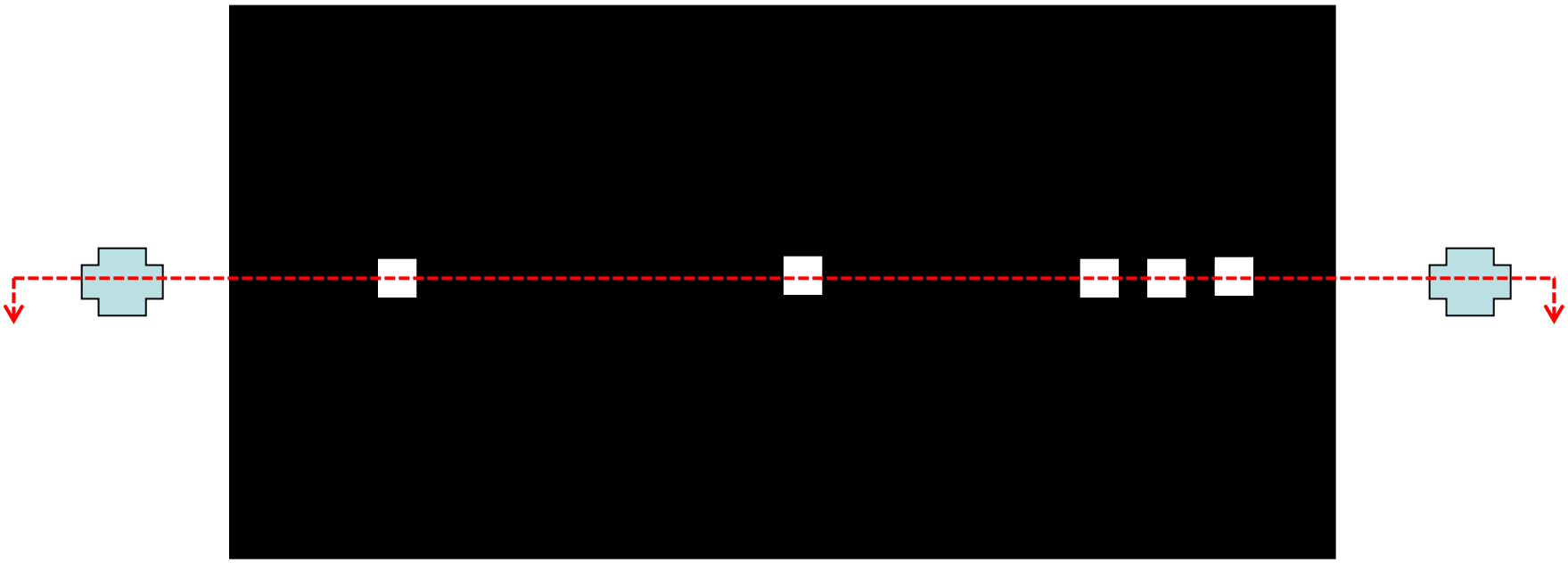
Metal-2 Interconnect Formation

- Metal 2: Ti/Al/TiN
- ILD-3 gap filling
- ILD-3
- ILD-polish
- Via-3 etch and via deposition, Ti/TiN/W

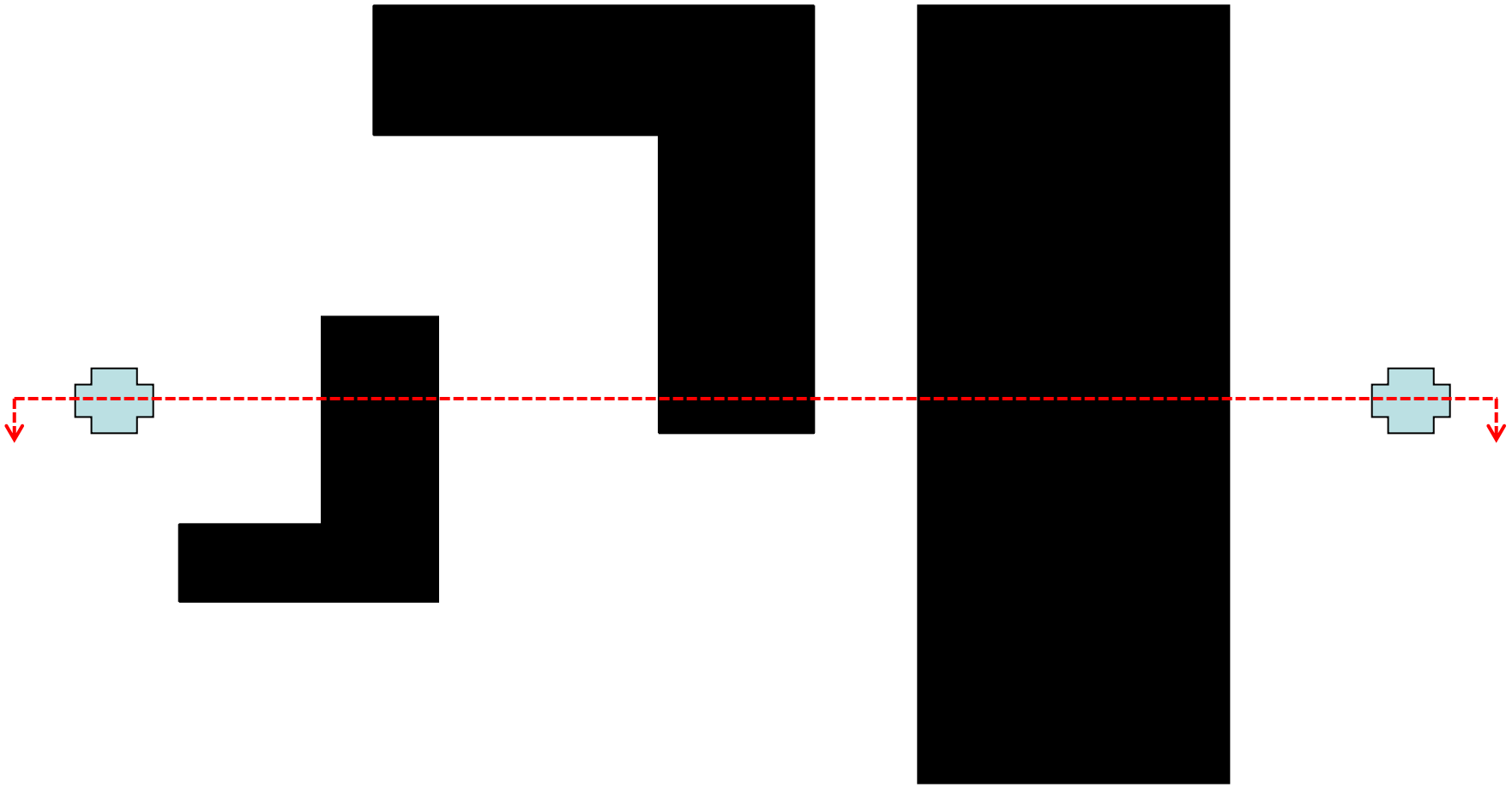




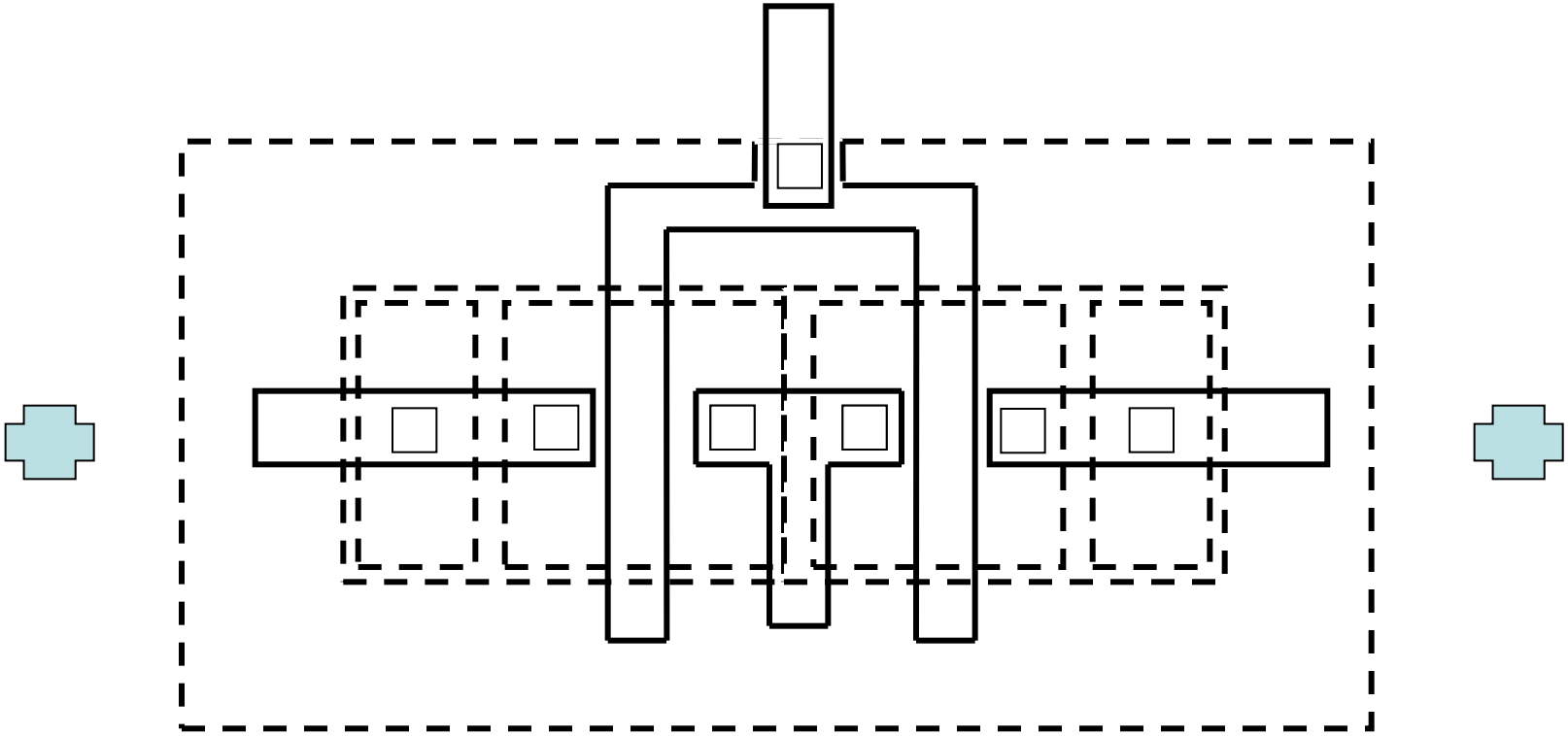
Mask # 13: Metal-2 formation



Mask # 14: Via-3 formation



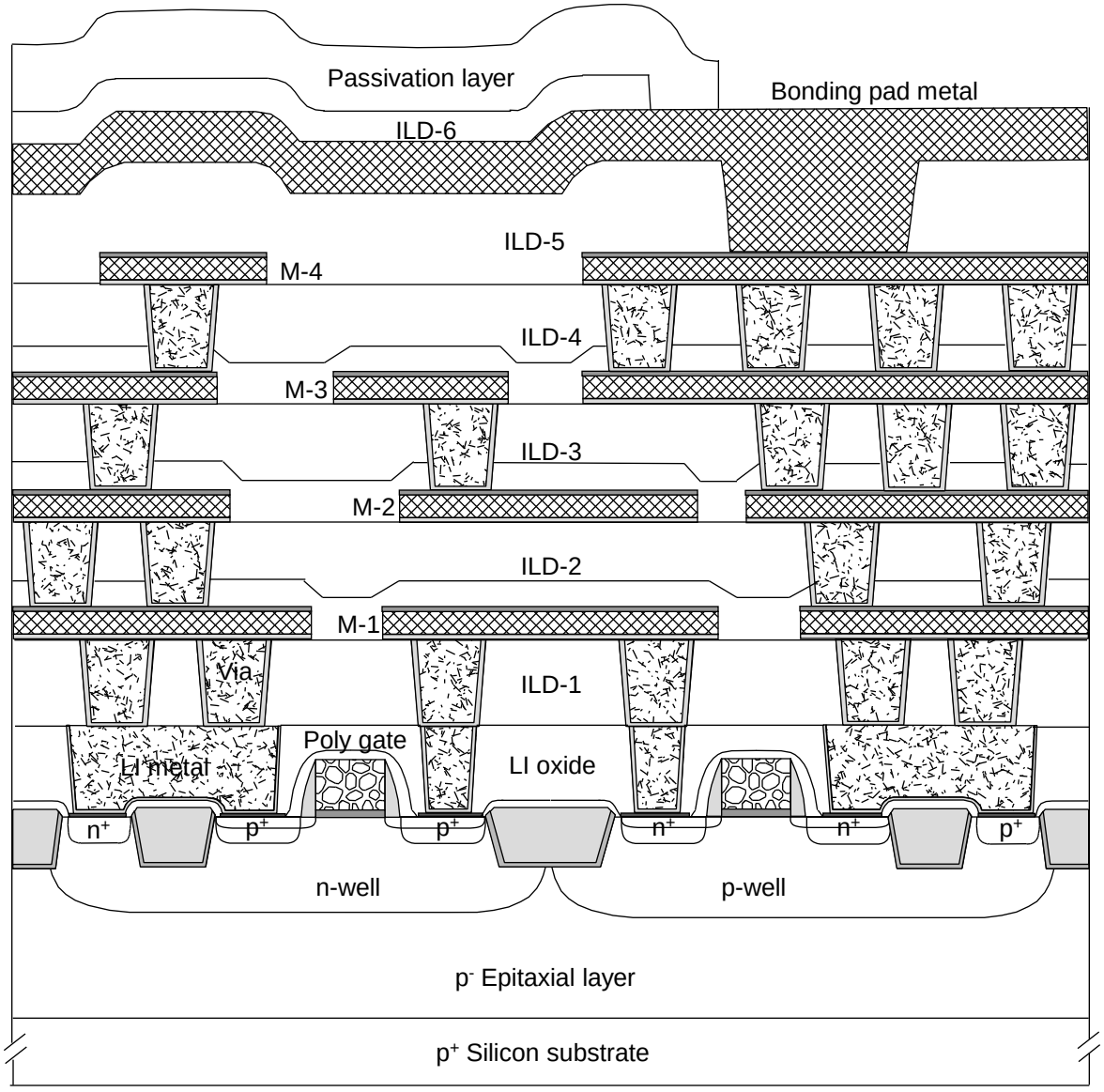
Mask # 15: Metal-3 formation



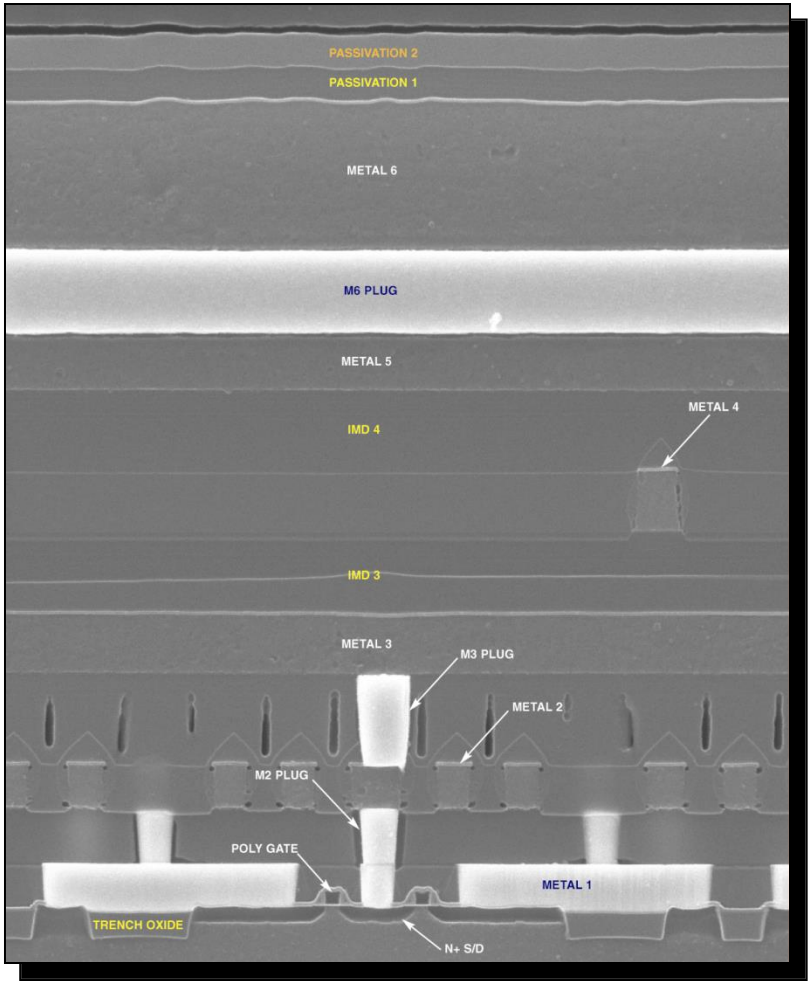
CMOS layout (mask 1 to mask 12)

Full 0.18 μm CMOS Cross Section

- Passivation layer of **nitride** is used to protect from moisture, scratched, and contamination
- ILD-6 : **oxide**



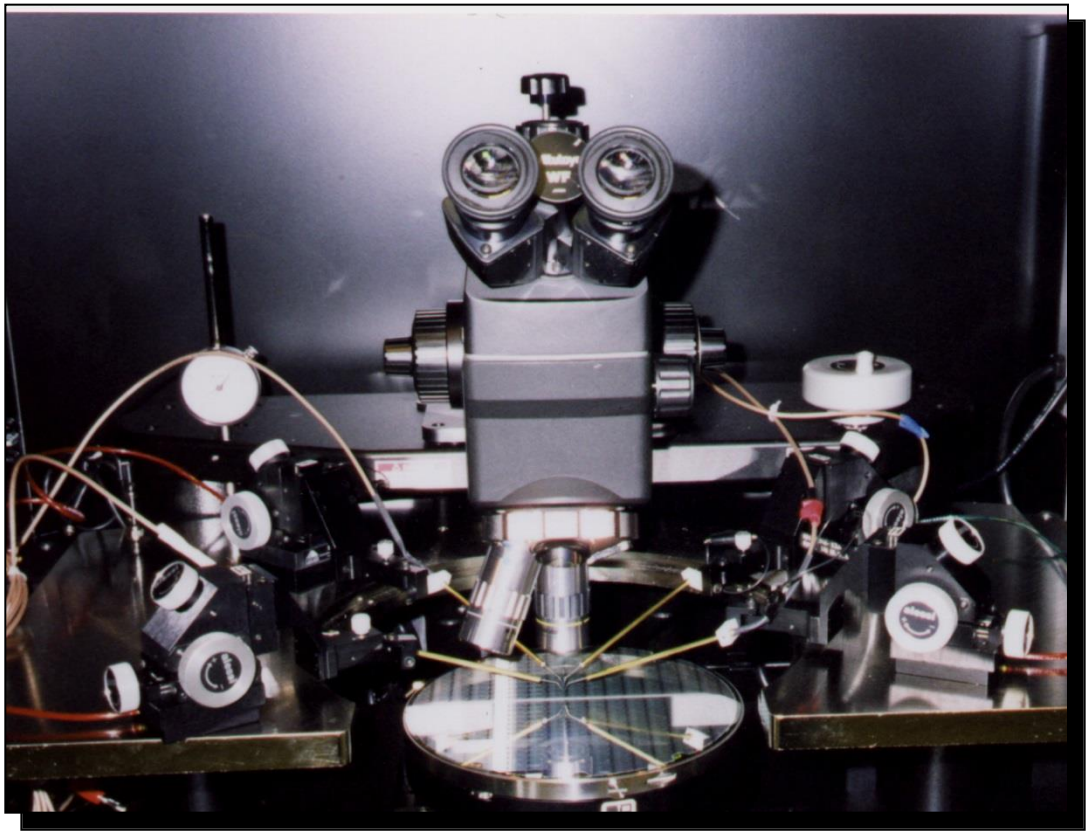
SEM Micrograph of Cross-section of AMD Microprocessor



Mag. 18,250 X

Micrograph courtesy of Integrated Circuit Engineering

Wafer Electrical Test using a Micromanipulator Prober (Parametric Testing)



- After metal-1 etch, wafer is tested, and after passivation test again
- Automatically test on wafer, sort good die (X-Y position, previous marked with an red ink)
- Before package, wafer is backgrind to a thinner thickness for easier slice and heat dissipation

Photo courtesy of Advanced Micro Devices