Design, fabrication and characterization of monolithic embedded parylene microchannels in silicon substrate†

Po-Jui Chen,*[a] Chi-Yuan Shih[a] and Yu-Chong Tai[ab]

Received 9th January 2006, Accepted 21st March 2006
First published as an Advance Article on the web 30th March 2006
DOI: 10.1039/b600224b

This paper presents a novel channel fabrication technology of bulk-micromachined monolithic embedded polymer channels in silicon substrate. The fabrication process favorably obviates the need for sacrifical materials in surface-micromachined channels and wafer-bonding in conventional bulk-micromachined channels. Single-layer-deposited parylene C (poly-*para*-xylylene C) is selected as a structural material in the microfabricated channels/columns to conduct life science research. High pressure capacity can be obtained in these channels by the assistance of silicon substrate support to meet the needs of high-pressure loading conditions in microfluidic applications. The fabrication technology is completely compatible with further lithographic CMOS/MEMS processes, which enables the fabricated embedded structures to be totally integrated with on-chip micro/nano-sensors/actuators/structures for miniaturized lab-on-a-chip systems. An exemplary process was described to show the feasibility of combining bulk micromachining and surface micromachining techniques in process integration. Embedded channels in versatile cross-section profile designs have been fabricated and characterized to demonstrate their capabilities for various applications. A quasi-hemi-circular-shaped embedded parylene channel has been fabricated and verified to withstand inner pressure loadings higher than 1000 psi without failure for micro-high performance liquid chromatography (μHPLC) analysis. Fabrication of a high-aspect-ratio (internal channel height/internal channel width, greater than 20) quasi-rectangular-shaped embedded parylene channel has also been presented and characterized. Its implementation in a single-mask spiral parylene column longer than 1.1 m in a 3.3 mm × 3.3 mm square size on a chip has been demonstrated for prospective micro-gas chromatography (μGC) and high-density, high-efficiency separations. This proposed monolithic embedded channel technology can be extensively implemented to fabricate microchannels/columns in high-pressure microfludics and high-performance/high-throughput chip-based micro total analysis systems (μTAS).

Introduction

From the last ten years, lab-on-a-chip concept has brought a lot of attention in life science, analytical chemistry, and biochemistry fields because chip-based miniaturized systems provide a vehicle to do faster (shorter operation time), more efficient (less sample consumption and higher sensitivity) analyses in smaller (hand-held system), cheaper (lower device and sample cost) platforms.[1] Various microfabricated components including channels, chambers, valves, pumps, mixers, filters, heaters, detectors can be integrated in a single chip substrate to perform fluid manipulation for analysis, and micromachined channels/columns are the most widely incorporated ones in the sense of delivering sample fluids among microdevices for separation/detection or even directly interacting with them by channel wall/fluid contact during delivery.[2] In order to serve as an alternative to off-chip silica-fused capillaries, on-chip channels are expected to have high biocompatibility, chemical inertness, mechanical strength, and flexibility of integration.[3] Silicon dioxide (SiO_2), glass, and polymers are then generally considered as on-chip channel structural materials.

Conventionally, based on target material of channel, microfabrication of on-chip channels can be sorted in two categories: (1) sacrificial-material-assisted suface-micro-machined channels;[4] (2) wafer-bonded bulk-micromachined channels.[2] As shown in Fig. 1(a), by coating/patterning a sacrificial layer (out of photoresist in case of microfabrication) and overcoating/patterning a device layer, the surface-micro-machined channels would be formed after stripping away the sacrificial layer at the end of process. Normally thin-film (poly-silicon, silicon oxide, silicon nitride, metals, and polymers) microchannels can be fabricated *via* this method.[5] Because the process does not affect integrity of the substrate, it provides great flexibility with respect to integrating other on-chip sensing/actuating devices. By using state-of-the-art surface micromachining processes, single-layer or multi-layer

[a]*Department of Electrical Engineering, Divison of Engineering and Applied Science, California Institute of Technology, Pasadena, CA, 91125, USA. E-mail: pjchen@mems.caltech.edu; Fax: +1-626-584-9104; Tel: +1-626-395-2254*
[b]*Department of Bioengineering, Division of Engineering and Applied Science, California Institute of Technology, Pasadena, CA, 91125, USA*
† Electronic supplementary information (ESI) available: Colour figures. See DOI: 10.1039/b600224b

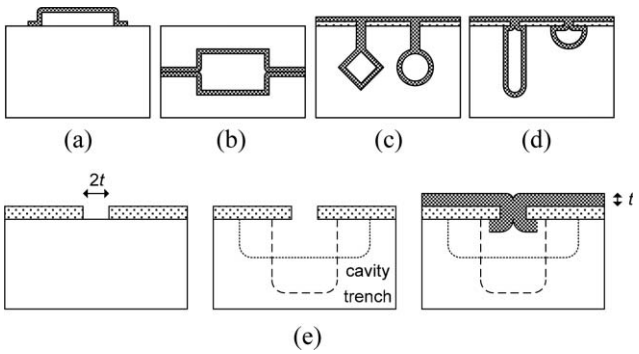

Fig. 1 Schematics of channel fabrication technologies: (a) surface-micromachined channel; (b) wafer-bonded channel; (c) buried channel; (d) embedded channel; (e) design of the proposed embedded channels in (d). As the final step, a conformal coating layer with thickness larger than t is necessary to seal the trench/cavity so an embedded channel is formed in the substrate.

integrated polymer micro-electro-mechanical-system (MEMS) devices have been successfully demonstrated in microfluidic applications with this fabrication technology.[6,7] With appropriate mechanical strengthening modification, surface-micromachined channels are also able to withstand high pressure loading in chip-based micro-high performance liquid chromatography (μHPLC).[8–10] Nevertheless, due to limitation of thickness control of the sacrificial layer in fabrication, the surface-micromachined channels can not have a large cross-section area, which corresponds to high flow resistance of such channels. Furthermore, because diffusion is the only mechanism of stripping sacrificial materials, the final stripping time needs to be sufficiently long, even on the scale of days or weeks, to completely evacuate those microchannels. It also implies an on-chip column longer than several centimetres would be difficult to fabricate. In addition, this type of channel is easily contaminated by residues of sacrificial materials inside channels. Effective and reliable cleaning of surface-micromachined channels is therefore an important issue. Fig. 1(b) shows the cross-section of a wafer-bonded bulk-micromachined channel. This fabrication technology is broadly used to fabricate SiO_2, glass, or polymer channels for high-throughput and efficient separations, specifically in micro-gas chromatography (μGC).[1,2,11–13] By performing bulk etching such as plasma reactive ion etching (RIE) or liquid-phase wet etching, trenches or cavities can be first created in a primary silicon/glass substrate. After being coated with target structural materials, the primary substrate is thermal-bonded or anodic-bonded to a secondary substrate having the same coating/structural material, which encloses a space and spontaneously forms encapsulated channels. Because the process does not require any sacrificial layer, residue contamination is completely eliminated, which implies metre-level-long channels can be fabricated without a problem. Channels with large cross-section area can also be built to have small flow resistance and resultant much higher volumetric flow rate. High pressure capacity is also applicable by the assistance of substrate support to withstand higher pressure loading than surface-micromachined channels.[1] However, bonding conditions in this fabrication need to be carefully characterized to get the optimized bonding strength. Challeges in the fabrication also include alignment and handling during bonding process, along with limitation of on-chip integration with surface-micromachined sensing/actuating components. In a way it would be a trade-off between off-chip coupling with other devices and miniaturization in lab-on-a-chip systems. Recently in the microbiochemistry field, under the similar bulk-micromachining concept, polymer molding techniques have been developed to rapidly and economically produce reaction channels,[14,15] but their employment in high-pressure applications and refined integrated microsystems remains questionable.

Beside the above two fabrication processes, consequently, a buried channel micromachining technology has been presented[16] to avoid the use of sacrificial materials while retaining its fabrication flexibility. As illustrated in Fig. 1(c), the process first creates trenches in a silicon substrate. While protecting only trench sidewalls by a passivation layer, the bottom of trench is further isotropically or anisotropically etched to create a pit larger than the original trench. After coating the structural material on the substrate in a conformal deposition, the trenches are sealed but their bottom pits are not because of their larger volume, so a buried channel is naturally formed. With a careful layout design, fluidic channel connections can be realized beneath the substrate surface. Although this bulk-micromachining technique has potential in 3-D microfluidic connection/network and on-chip integration with surface-micromachined components due to no need of wafer-bonding, the fabricated channels have difficulty in obtaining high performance compared to wafer-bonded channels because the geometrical profile and cross-section area of buried channels are limited from the complexity of process control and micromachining bottom of trenches without affecting the morphology of trench sidewalls. Other than the buried channel process, it is worth noting that the bulk-etched grooves/trenches can also be enclosed by using thin-film deposition through top perforated membranes to form channels.[17] While it needs to be further explored, this method has the capacity to build microfluidic channels with appropriate modification.

In order to provide a total solution to all the mentioned issues in existing fabricated channels, a novel method for formation of channels, embedded (one-side buried) channel technology, as shown in Fig. 1(d), is therefore proposed in this paper. It inherits advantages of bulk-micromachined channels such as withstanding high-pressure loading and no need of sacrificial materials, while it does not require a wafer-bonding process. Because of the fabrication method, the design of embedded channels is much more flexible than that of buried channels and surface-micromachined channels, hence it gives the channels more degrees of freedom in their cross-section profiles to accommodate functions including long-channel, high-pressure, or high-flow-rate operations. Moreover, the fabrication is completely compatible with further lithographic CMOS/MEMS processes, which facilitates integration with other on-chip devices. Here by using a polymer structural material through silicon micromachining processes, design, fabrication, and characterization of monolithic embedded channel technology were described to show its feasibility. Cleaner, more flexible, and more robust channels fabricated by

this technology were also implemented for prospective chip-based μHPLC and μGC to show their capabilities in microfluidic and lab-on-a-chip devices.

Design

The design of embedded channels is fairly straightforward. In the process illustrated in Fig. 1(e), a thin film is first deposited and patterned on the substrate to serve as a hard etch mask. At this step the layout of channels is also determined with a small characteristic opening width $2t$. From those exposed regions on surface, trenches or cavities can be created by bulk etching of the substrate. Due to the etching selectivity of materials the etch mask is hardly etched, which results in mask overhang on top of trenches/cavities. By controlling the process of bulk etching, trenches/cavities wider than $2t$ in different geometrical shapes are obtained in order to leave a space beneath substrate surface for embedded channels. Finally, by coating structural material on the substrate in a conformal deposition, the $2t$ opening in between mask overhang is totally sealed when the deposition thickness is greater than t, while embedded channels with thickness t are concurrently formed at trenches/cavities in substrate. These channels are fully enclosed except for fluidic access ports in which the exposed openings were originally greater than $2t$. By implementing this design, the embedded channels can be micromachined by using a single mask and single device layer deposition, and the process does not require sacrificial material stripping or wafer bonding as in conventional channels. Because of high flexibility given by the fabrication technology, versatile designs of embedded channels can be accomplished and implemented for various applications.[18–20]

For structural material selection, any material that can be conformally deposited on a substrate is a candidate to construct embedded channels. Parylene C (poly-*para*-xylylene C) is selected as the structural material on account of its desirable properties such as high mechanical flexibility (Young's modulus $\approx$ 4 GPa), chemical inertness to organic and inorganic solvents, biocompatibility (FDA approved USP Class VI grade), and transparency (small light absorption in the visible region).[21] The coating of parylene features a pinhole-free conformal chemical-vapor-deposition (CVD) process at room temperature, which is completely compatible with other microfabrication technologies and enables final trench/cavity sealing in fabrication of the embedded channels. Recently, parylene C has been extensively used as a primary material in MEMS in the area of microfluidics, bioMEMS, and chip-based micro-total-analysis systems (μTAS).[22,23] The rest of this paper exploits single-layer-deposited parylene C as a promising polymer material to demonstrate details of the embedded channel fabrication and applications.

Experimental

Fabrication of quasi-hemi-circular embedded channels

This section describes the fabrication of quasi-hemi-circular monolithic embedded channels. The process illustrated in Fig. 2(a) started with growing a 0.5 μm thermal oxide on a standard 4-inch silicon wafer. Through a photoresist mask, the oxide was patterned by using buffered hydrofluoric acid (BHF) to define layout of the channels. After oxide patterning, a customized xenon difluoride (XeF_2) gas-phase silicon etching system[24] was used to isotropically etch exposed silicon. Depending on the oxide opening size, up to 40 μm silicon undercut was created beneath the oxide etch mask after 18 loops of XeF_2 etching. Finally, a 15 μm thick parylene C layer was conformally deposited on the wafer in a Cookson Electronics™ PDS system (Specialty Coating Systems Inc., Indianapolis, IN). The parylene coating completely sealed the oxide opening on top of the etched cavities so that embedded channels were formed. Fig. 2(b) shows a micrograph of the fabricated single-mask, single-layer, quasi-hemi-circular monolithic embedded parylene channel.

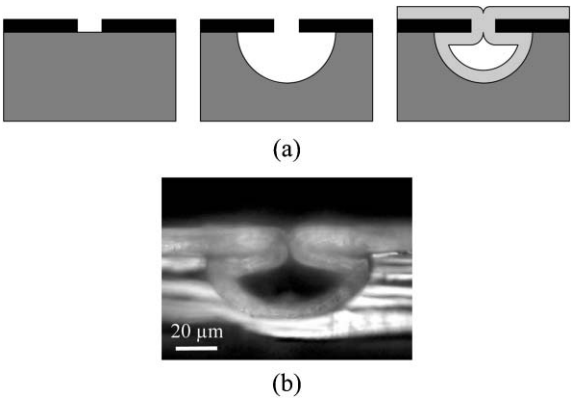

Fig. 2 Quasi-hemi-circular embedded channel fabrication process: (a) process flow; (b) micrograph of the fabricated channel (cross-section view).

In this process, ideally, the bulk-etched silicon should have isotropic undercut to perfectly form hemi-circular embedded channels. However, due to mass transport and loading effect phenomena in XeF_2 etching, the silicon etch rate was not constant but a function of exposed silicon area and direction of etching. Fig. 3 shows that, within a range of oxide opening widths, larger oxide openings led to a larger XeF_2-etched cavity cross-section. In addition, the silicon etch rate in the vertical direction was larger than that in the horizontal

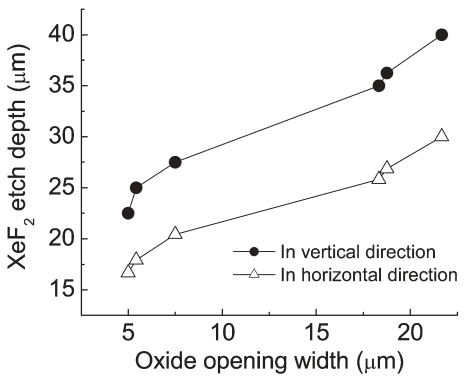

Fig. 3 Characterization of XeF_2 etching in quasi-hemi-circular embedded channel fabrication. This plot illustrates the data after 18 loops of XeF_2 etching performed to the silicon wafer.

direction. It implies a perfect hemi-circular cross-section of embedded channel is difficult to obtain by using XeF_2 etching. If one would like to fabricate channels with perfect hemi-circular profiles, HNA (a mixture of HF, HNO_3, and CH_3COOH) or other wet etchant is preferred even though a more robust masking layer than thin oxide layer may be required.[25] Data in Fig. 3 also indicates that by controlling the oxide opening width, the resultant cross-section area of XeF_2-etched embedded channels is varied. This effect can be applied to create a single channel consisting of sections having different functions, as shown in supplementary data†. For example, a separation column (large oxide opening width, large channel cross-section) and a bead filter (small oxide opening width, small channel cross-section) can be fabricated in the same channel line. Moreover, after the oxide opening around the filter section was sealed by parylene deposition, the size of the filter cross-section continued to shrink because of parylene overcoating to its inner surface through neighboring oxide opening of the column section in the same channel. This mechanism facilitates the formation of a more contracted hence more selective filter. Using deliberate oxide opening size difference, fluidic inlet/outlet ports were made at assigned places having much larger areas of exposed silicon so they were not sealed by parylene coating. This fabrication technique enables that an entire microfluidic system including column/filter/port structures can be fabricated on a chip without assembly requirements.

Fabrication of high-aspect-ratio quasi-rectangular channels

Among manifold geometrical designs, high-aspect-ratio (HAR) rectangular cross-sectioned channels have a remarkable capability for promoting strong chemical interactions between sample fluids and channel walls, where chemical interactions, catalysis, or exchange occurs.[26,27] Low flow resistance resulting from the channel profile also facilitates high volumetric flow rate, which makes it possible that the channel length can be further increased without excessively increasing the injection pressure for maintaining reasonable fluidic flow rate and analysis time.[5] HAR channels are generally micromachined in a vertical paradigm to have a high density of channels per unit area on a chip and therefore provide a long vertically-accumulated absorption path length for optical detection.[1] HAR embedded channels would have quite a few advantages over wafer-bonded and buried channels, but used to come with a crucial challenge – producing rectangular HAR trenches underneath overhanging etch mask for a following conformal layer deposition to seal them. HAR trenches with uniform sidewall undercut are necessary in this process, while the fabrication is conventionally difficult due to mass transport limitations in successive sidewall etching which leads to a non-ideal "vase-like" undercut profile.[28] Correspondingly, described below, a novel two-step trench etching technique is developed and implemented to overcome the challenge and fabricate reliable monolithic HAR rectangular embedded channels.

The fabrication process illustrated in Fig. 4(a) began with 0.5 μm wet oxidation as a etch mask on a standard 4-inch silicon wafer. A 10 μm thick AZ4620 photoresist (Clariant

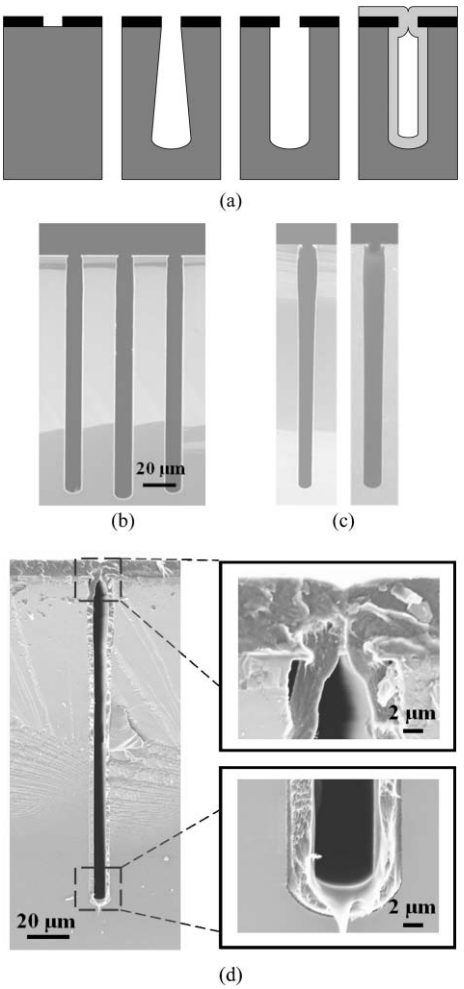

Fig. 4 HAR quasi-rectangular embedded channel fabrication process: (a) process flow; (b) SEM image of trenches after first-step re-entrant DRIE etching; (c) SEM image of trenches after second-step complementary dry etching, including SF_6 plasma etching (left) and XeF_2 gas-phase etching (right). Note the oxide overhang on top of trenches; (d) SEM images of microfabricated monolithic HAR quasi-rectangular embedded parylene channel (left) and its cut-views (right).

Corp., Charlotte, NC) layer was then spun on the wafer for two purposes: (1) patterning the oxide; (2) protecting the oxide during the following trench etching. This two-layer etch mask can effectively both minimize the necessary oxide thickness and avoid photoresist erosion effects during later plasma etching. Through this photoresist mask, the oxide was patterned by using BHF to define the layout of the channel. After that a two-step complementary etching was directly performed. First, plasma-assisted deep reactive ion etching (DRIE) was exploited to achieve initial HAR trench etching. By controlling time-multiplexed periods of fluorine-based SF_6 etching and C_4F_8 polymerization (passivation layer coating) in Bosch process of DRIE, re-entrant (negative-tapered) trenches can be intentionally realized with a designated slope.[29] For a 6.5 μm oxide mask opening, after 200 loops of modified Bosch process with multiplexed 14 s SF_6 etching and 5 s C_4F_8 polymerization in a PlasmaTherm™ DRIE system (Unaxis

Inc., St. Petersburg, FL), a 155 μm deep trench with 3.5 μm side undercut on the bottom was created in the silicon substrate as shown in Fig. 4(b). Subsequently, the trenches were dry-etched to obtain positive-sloped undercut from the top in order to complement rectangular cross-section profile for the following structural layer deposition. In this step SF_6 plasma etching and XeF_2 gas-phase etching were selected to perform the second-step dry etching. SEM images in Fig. 4(c) show that both etching methods have demonstrated their capability for creating quasi-rectangular (sidewall angle 90° within ±1° variation) trenches with 2.5 μm oxide overhang. After stripping the photoresist with acetone, an 8 μm thick parylene C layer finally coated the substrate and enclosed the trenches to construct embedded channels. The thickness of the parylene C layer was larger than two times the characteristic oxide opening to ensure the trenches were completely sealed. Fig. 4(d) shows SEM cross-section images of the micro-machined monolithic HAR quasi-rectangular embedded parylene channel with internal aspect ratio (internal channel height/internal channel width) around 23. It is believed that this value can increase further to 30, which approaches the ultimate limit of the Bosch process in state-of-the-art DRIE systems. The top close-up image of the channel in Fig. 4(d) also shows that, even when the thickness of parylene C coating was more than necessary, the excessive parylene would deposit only on top of the channels and not on the sidewalls after the channels were sealed. This fact greatly reduces the complexity of controlling thickness and uniformity of parylene C coating in fabrication of the HAR channels.

In this process, apparently, the first-step DRIE trench etching is the key to channel fabrication. Fig. 5(a) illustrates, for a 6.5 μm oxide mask opening, the relationship of average silicon etch rate and re-entrant trench slope as a function of SF_6 etch time during one Bosch loop after 200 loops of etching. It indicates that both etch rate and etch slope increase linearly with a increased SF_6 etch time from 7 s to 14 s, which are typical numbers in the Bosch process.[3] Beyond this time range, it would turn out that the C_4F_8 polymerization layer on the bottom of the trench could not be completely removed after relatively short SF_6 plasma etching, which affects the formation of deep trenches. On the other hand, the C_4F_8 passivation layer on the sidewalls of the trench could be completely removed after relatively long SF_6 etching, which affects the morphology of the trench profile. By understanding the interactions between SF_6 and C_4F_8 plasma and hence carefully tuning them along with other parameters (*e.g.*, chamber pressure, electrode temperature, *etc.*), the proposed technique can be universally accomplished in every DRIE system.

Because this process heavily depends on plasma reactions, its characterization requires more study on rendering influences of mass tranport and loading effect phenomena in the first-step DRIE trench etching. Fig. 5(b) and Fig. 5(c) show that, in different oxide mask opening widths, the relationship of average silicon etch rate and re-entrant trench slope as a function of SF_6 etch time during one Bosch loop after 150 loops of etching. It indicates that within a opening range, larger amounts of silicon would be etched in larger exposed area of silicon, which causes deeper trenches for the same SF_6 plasma etch time. However, it was observed that, regardless of the different oxide opening widths, the bottom undercut of the trenches was approximately the same under the same SF_6 etch time, which caused a smaller trench etch slope in a larger oxide opening region. This size effect needs to be considered when processing the HAR embedded channels.

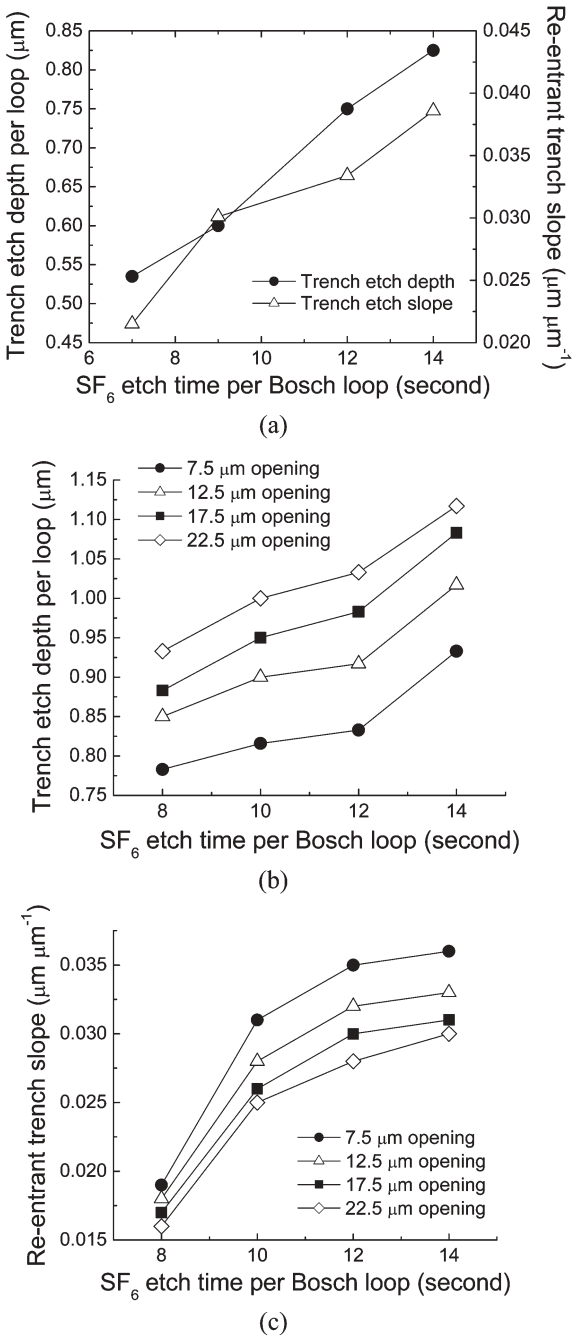

Fig. 5 Characterization of re-entrant DRIE etching: (a) relationship of trench etch depth and negative-tapered etch slope as a function of SF_6 etch time during one loop in the modified Bosch process; (b) size effect of trench etch depth with different oxide opening widths; (c) size effect of negative-tapered etch slope with different oxide opening widths. Decreased etch slope in increased oxide openings results from the same sidewall undercut on bottom of trenches regardless of different openings.

Process integration with surface micromachining

After conformal deposition of structural material on the substrate, the substrate surface is supposed to be planarized because the original openings are sealed to construct embedded channels. Fig. 2(b) and Fig. 4(d) show that surfaces above the channels were qualitatively flat after fabrication. This outcome guarantees the availability of further lithographic processes on the substrate consisting of embedded channels. An exemplary process in bulk-micromachining/surface-micromachining combination was designed to verify the concept.

The fabrication process flow is illustrated in Fig. 6(a). Started with the processed silicon wafer having parylene HAR quasi-rectangular embedded channels, a 15 μm thick AZ4620 photoresist layer was used as a mask to pattern the parylene channel layer by using oxygen plasma. After BHF oxide removal, a 20 μm thick AZ4620 photoresist layer was spun on the wafer and patterned to be the sacrificial material. An additional 10 μm thick parylene C layer was then deposited on the wafer. With a 40 μm thick AZ4620 photoresist mask layer, the parylene was patterned by using oxygen plasma to transfer the design features. Finally, after photoresist stripping with acetone, a 10 μm thick perforated parylene membrane suspended on top of HAR embedded parylene channels with a 20 μm high gap was substantially formed. As shown in Fig. 6(b), through openings of the parylene membrane, the wafer surface consisting of parylene embedded channels were still exposed to outside, allowing the thin-walled parylene channels to be dry-released after XeF_2 gas-phase silicon etching. As a matter of fact, the parylene membrane was intact even after channel release. It demonstrated not only exceptional chemical resistance of parylene C but successful bulk-micromachining/surface-micromachining integration. This process provides evidence that the presented channel fabrication technology facilitates on-chip integration with micro/nano-sensors/actuators/structures *via* regular CMOS/MEMS lithographic processes.

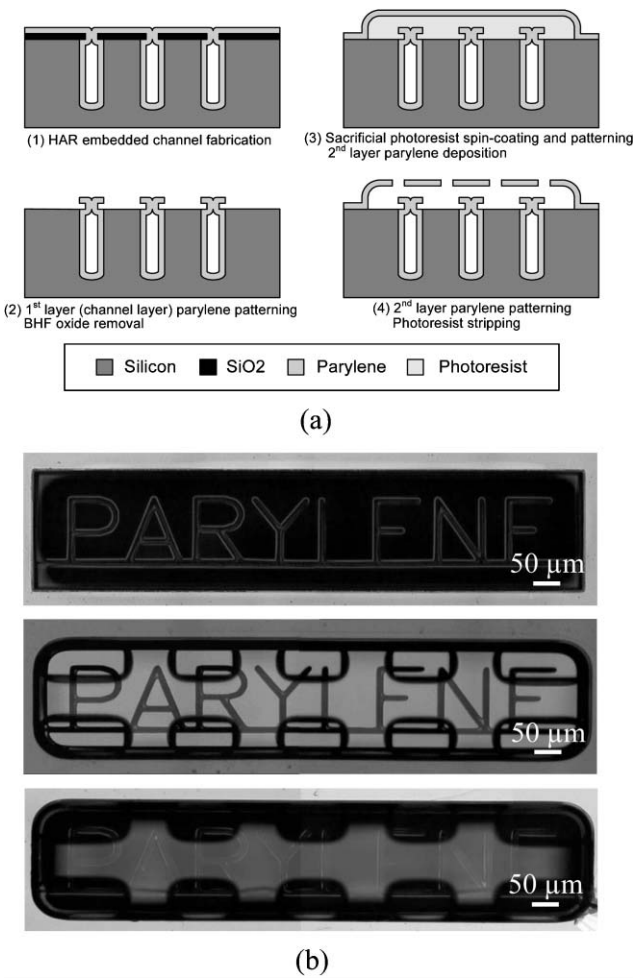

Fig. 6 Bulk-micromachining/surface-micromachining integration: (a) process flow. Final XeF_2 silicon etching step is not shown in schematics; (b) micrographs for demonstrating process integration (top-view): (top) dry-released HAR thin-walled channels after XeF_2 silicon etching. (middle) Fabricated perforated parylene membrane on top of embedded channels before channel release. The text "PARYLENE" is visible due to the transparency of parylene C. (bottom) The channels and the membrane after dry release. The perforated parylene membrane was intact after XeF_2 silicon etching.

Results and discussion

With the developed channel fabrication technology, devices featuring quasi-hemi-circular embedded parylene channels and HAR quasi-rectangular embedded parylene channels were monolithically fabricated in a silicon substrate to demonstrate their functionality for potential applications in microfluidics and chip-based separation and analysis. In order to establish a microscale/macroscale fludic interface for device testing, a customized jig similar to those in the literature[9,10] and Upchurch™ fittings (Upchurch Scientific Inc., Oak Harbor, WA) were utilized to set up interface couplings and connections.

For quasi-hemi-circular embedded channels, the fabricated column as shown in Fig. 2(b) was first used to perform preliminary pressure testing. Stress distribution in inner-pressurized parylene channels was analyzed by FEMLAB™‡ simulation (Comsol Inc., Los Angeles, CA) to estimate the performance of embedded channels in high-pressure loading conditions. Simulation results, as shown in supplementary data†, verified that embedded-channel boundary conditions effectively reduce the maximum stress by 34% compared to freestanding-channel boundary conditions, implying a higher pressure loading can be applied to embedded channels compared with freestanding channels, which is more beneficial to high-pressure separation-bead packing. Maximum pressure capacity of the fabricated test structure was experimentally studied using nitrogen gas as a pressure source. The maximum pressure capacity was determined by the pressure loading at which a closed column failed to hold the enclosed fluids such that leakage happened thereafter. Fig. 7 indicates that the embedded parylene channel can withstand at least 1000 psi pressure loading without any observable flow leakage. In addition, the low gas permeability of parylene C[21] guarantees

‡ FEMLAB™ has been named COMSOL Multiphysics™ after the release of FEMLAB™ version 3.2.

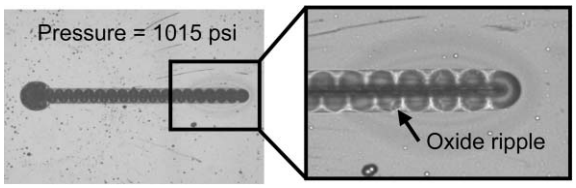

Fig. 7 Micrographs of the embedded parylene channel after loading with 1015 psi inner pressure (left) and its close-up (right). Oxide ripples were observed due to their large deformation from multi-layer stress distribution.

the column can be maintained at such a high pressure without long-term gas permeation/leakage. The testing results demonstrated a significant breakthrough in terms of microfludic channel pressure capacity, which is crucial for chip-based chromatography applications and challenging with conventional surface-micromachined channel technology. Implementing this type of embedded channels, a monolithic embedded HPLC system consisting of a separation column, a stationary-phase bead filter, fluidic inlet/outlet ports, and an optical detection cell was successfully fabricated on a chip, as shown in supplementary data†. With an optimized filter structure, 5 μm fluorescent beads were successfully packed into the fabricated separation column *via* slurry-packing technique under 200 psi packing pressure. Supplementary data† show the fluorescence image of packed beads in the column. It is observable due to the fact that parylene channel walls have good transparency to visible light as stated before.

For high-aspect-ratio quasi-rectangular embedded parylene channels, with implementation of the micromachined channel, a single-layer spiral parylene separation column longer than 1.1 m with front-side fluidic inlet/outlet ports was successfully fabricated with single mask in a 3.3 mm × 3.3 mm square size on a chip as shown in supplementary data†. As expected, the visible-light transparent property of parylene C provides the column the availability of having optical detection such as fluorescence imaging for analysis. Moreover, the sensitivity of optical detection in this type of channel is greatly enhanced due to in-plane signal accumulation from projected light in vertically HAR channels. Besides, the advantageous characteristics such as high pressure capacity, low fluidic resistance, and high density (channel length per unit area on a chip) of HAR embedded channels realize high-efficiency and high-throughput chip-based separation. As a result, such an embedded parylene channel/column can be incorporated as a prospective element in high-performance μGC and other high-throughput separation and analysis.

Conclusion

A novel channel fabrication technology has been presented to produce embedded (one-side buried) polymer microchannels in silicon substrate. Unlike conventional surface-micromachined and bulk-micromachined channels, embedded channels compromise merits as being both monolithically fabricated and free from sacrificial material usage. These key factors enable the micromachined channel to be long, high-density, and free from process residue contamination. High pressure capacity can be obtained from these channels by the assistance of substrate support. Parylene C was selected as the channel structural material because of its favorable mechanical, optical, chemical, and biomedical properties. Fully-dry etching techniques and single-layer conformal parylene deposition were employed to construct various cross-section shapes of embedded channels, including quasi-hemi-circular and high-aspect-ratio quasi-rectangular profiles, in a silicon wafer. Fabrication results have successfully demonstrated the feasibility of the proposed technology, along with its compatibility of integration with lithographic CMOS/MEMS post-processes. Devices featuring embedded parylene channels in silicon substrates have been fabricated and characterized. Testing results have demonstrated and verified embedded parylene channels as prospective elements in chip-based μHPLC, μGC, and other high-pressure, high-efficiency, high-throughput μTAS applications. These microfabricated monolithic embedded parylene channels can be extensively implemented in microfluidic and lab-on-a-chip systems in the scope of conducting life science, analytical chemistry, and biochemistry researches.

Acknowledgements

This work was supported in part by the Engineering Research Centers Program of the National Science Foundation under NSF Award Number EEC-0310723 and EEC-9402726. The authors would like to especially thank Mr Damien Rodger for his valuable comments as well as Mr Trevor Roper for his fabrication assistance.

References

1 A. v. d. Berg and T. S. J. Lammerink, *Top. Curr. Chem.*, 1998, **194**, 21–49.
2 G. Lambertus, A. Elstro, K. Sensenig, J. Potkay, M. Agah, S. Scheuering, K. D. Wise, F. Dorman and R. Sacks, *Anal. Chem.*, 2004, **76**, 2629–2637.
3 M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization*, 2nd edn, CRC Press, Boca Raton, FL, USA, 2002.
4 M. A. Burns, B. N. Johnson, S. Brahmasandra, K. Handique, J. Webster, M. Krishnan, T. Sammarco, P. Man, D. Jones, D. Heldsinger, C. Mastrangelo and D. Burke, *Science*, 1998, **282**, 484–487.
5 G. T. A. Kovacs, *Micromachined Transducers Sourcebook*, McGraw-Hill, Boston, MA, USA, 1998.
6 J. Xie, J. Shih and Y.-C. Tai, *Technical Digest, The 16th IEEE International Conference on MicroElectroMechanical Systems (MEMS 2003)*, Kyoto, Japan, 19th–23rd Jan., 2003, pp. 20–23.
7 J. Xie, J. Shih, Q. Lin, B. Yang and Y.-C. Tai, *Lab Chip*, 2004, **4**, 405–501.
8 J. Xie, Y. Miao, J. Shih, Q. He, J. Liu, Y.-C. Tai and T. D. Lee, *Anal. Chem.*, 2004, **76**, 3756–3763.
9 Q. He, C. Pang, Y.-C. Tai and T. D. Lee, *Technical Digest, The 17th IEEE International Conference on MicroElectroMechanical Systems (MEMS 2004)*, Maastricht, The Netherlands, 25th–29th Jan., 2004, pp. 212–215.
10 C.-Y. Shih, Y. Chen, J. Xie, Q. He and Y.-C. Tai, *Sens. Actuators, A*, 2006, **127**, 207–215.
11 P. Mao and J. Han, *Lab Chip*, 2005, **5**, 837–844.
12 H.-S. Noh, P. J. Hesketh and G. C. Frye-Mason, *J. Microelectromech. Syst.*, 2002, **11**, 718–725.
13 S. C. Terry, J. H. Jerman and J. B. Angell, *IEEE Trans. Electron Devices*, 1979, **26**, 1880–1886.
14 E. Kim, Y. N. Xia and W. M. George, *Nature*, 1999, **376**, 581–584.

15 H.-S. Noh, Y. Huang and P. J. Hesketh, *Sens. Actuators, B*, 2004, **102**, 78–85.
16 M. J. d. Boer, R. W. Tjerkstra, J. W. Berenschot, H. V. Jansen, G. J. Burger, J. G. E. Gardeniers, M. Elwenspoek and A. v. d. Berg, *J. Microelectromech. Syst.*, 2000, **9**, 94–103.
17 C. Vieider, J. Holm, L. Forssen, H. Elderstig, S. Lindgren and H. Ahlfeldt, *Technical Digest, The 9th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers 1997)*, Chicago, IL, USA, 16th–19th June, 1997, pp. 679–682.
18 C.-Y. Shih and Y.-C. Tai, *Technical Digest, The 9th International Conference on Miniaturized Systems for Chemistry and Life Sciences (MicroTAS 2005)*, Boston, MA, USA, 9th–13th Oct., 2005, pp. 343–345.
19 P.-J. Chen, D. Rodger and Y.-C. Tai, *Technical Digest, The 9th International Conference on Miniaturized Systems for Chemistry and Life Sciences (MicroTAS 2005)*, Boston, MA, USA, 9th–13th Oct., 2005, pp. 181–183.
20 M. Agah and K. D. Wise, *Technical Digest, The 18th IEEE International Conference on MicroElectroMechanical Systems (MEMS 2005)*, Miami Beach, FL, USA, 2005, pp. 774–777.
21 Cookson Special Coating Systems, http://www.scscoatings.com/parylene_knowledge/specifications.cfm.
22 Y.-C. Tai, *Technical Digest, IEEE International Conference on Robotics and Biomimetics (ROBIO)*, Hong Kong SAR and Macau SAR, China, 29th June–3rd July, 2005.
23 Y.-C. Tai and C.-M. Ho, *Technical Digest, The 6th Symposium on Smart Control of Turbulence*, Tokyo, Japan, 6th–9th May, 2005.
24 X. Q. Wang, X. Yang, K. Walsh and Y.-C. Tai, *Technical Digest, The 9th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers 1997)*, Chicago, IL, USA, 16th–19th June, 1997, pp. 1505–1508.
25 K. R. Williams and R. S. Muller, *J. Microelectromech. Syst.*, 1996, **5**, 256–269.
26 P. M. Martin, D. W. Matson and W. D. Bennett, *Chem. Eng. Commun.*, 1999, **173**, 245–254.
27 G. E. Spangler, *J. Microcolumn Sep.*, 2001, **13**, 285–292.
28 P.-J. Chen, D. C. Rodger, M. S. Humayun and Y.-C. Tai, *Sens. Actuators, A*, 2006, **127**, 276–282.
29 K.-S. Chen, A. A. Ayon, X. Zhang and S. M. Spearing, *J. Microelectromech. Syst.*, 2002, **11**, 264–275.

