Materials Research Express

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To cite this article before publication: Shui-Hsiang Su *et al* 2020 *Mater. Res. Express* in press https://doi.org/10.1088/2053-1591/ab7c84

Enhancing reliability of InGaN/GaN light-emitting diodes by controlling the etching profile of the current blocking layer

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Abstract

SiO_2 was used as the current blocking layer (CBL) during fabricating the InGaN/GaN-based light-emitting diodes (LEDs). The SiO_2 film was prepared by plasma enhanced chemical vapor deposition (PECVD) at a lower temperature (LT) of 180℃ and a higher temperature (HT) of 280℃ for characterizing the reliability of LEDs. The degradation of output power in LT-CBL LED is as high as 6.8% during 1000 hours in the high-temperature and humidity (85℃/85 RH) condition. Experimental results demonstrate the low temperature grown CBL forms a larger side-wall angle via wet etching. The thinner side-wall ITO film cracks and the current spreading effect is suppressed, causing drastic power degradation. On the contrary, the HT-CBL SiO_2 demonstrates optimal step coverage of ITO film for current spreading and then the HT-CBL LEDs slightly degrade as low as 5% in the accelerated reliability test. A dense quality of HT-CBL SiO_2 as well as a good CBL decreased parasitic optical absorption in the *p*-pad electrode and *p*-finger. Besides, the HT-CBL SiO_2 showed a small side-wall angle of 40° which increased the step coverage and current spreading of ITO. An approach is conducted to confirm the side-wall profile of CBL for each process.

KEY WORDS: LED, GaN, current blocking layer

1. Introduction

InGaN/GaN-based light-emitting diodes (LEDs) have been regarded as the promising candidate for lighting technology because of their application in back lighting, full-color display, and traffic signals [1-4]. Many groups had investigated for high power LEDs, which also has a remarkable growth in the solid-state lighting. Nevertheless, InGaN/GaN-based LEDs exist the limited light extraction efficiency due to the total internal reflection between GaN (n=2.5) and air (n=1). According to Snell's law, the critical angle (θ c) is only around 23˚, the result indicates that the photons can only escape from GaN to air within 23˚[5,6]. In addition, the limit of internal quantum efficiency (IQE) of LEDs is almost as up to 90%. The other difficult issues have been show such as strong piezoelectric in quantum wells and low hole concentration of Mg-doped GaN. Therefore, in order to improve the light extraction efficiency of InGaN/GaN-based LEDs, there are several groups have reported the methods for reduced the total internal reflection and enhanced the output power, such as pattern structure [7,8], V-shaped pits [9,10], reflective current blocking layer [11,12], and photonic crystal [13]. In particular, for conventional LED the high resistivity in *p*-GaN:Mg would restrict the lateral current spreading, leading the non-uniform emission distribution in indium-tin-oxide (ITO) layer and casing current crowding effect in the LED structure. Many methods were used to investigate in current blocking layer (CBL) and its stack layer arranged, for alleviating the photons emission from multiple quantum wall (MQW) active layer would be absorbed under pad region. Hence, the investigations in material application on CBL were including the Ag or Al particles embedded within SiO_2 layer as reflector to reduce the photons through under pad area [14,15], O_2 plasma-treated current blocking region to prevent the emission absorbed via metal pad [16], a line-width simulation in CBL [17] and a newly material InZnO as schottky blocking layer [18], Mg implantation into invisible CBL to decrease the current crowding effect of emission region [19]. However, as of now there seem not to have discussion the etching mechanism and side-wall profile with different grown temperature for SiO_2 as CBL. Since the side-wall angle of CBL would influence ITO side-wall profile and lead to the poor step coverage of ITO, it might result in an unstable optical property in reliability of LED device.

In this work, we have fabricated InGaN/GaN-based LEDs using SiO_2 as a CBL. SiO_2 is prepared by plasma enhanced chemical vapor deposition (PECVD) at 180°C and 280°C. The side-wall profile of SiO_2 and related etching mechanism are discussed. The performance of CBL is characterized depending on the observation of film's quality. Finally, we investigate the reliability of LEDs under the accelerated reliability test.

2. Experimental

Figure 1 schematically illustrates the LED structure. GaN-based LED with a 30 nm-thick GaN nucleation layer at the temperature of 550℃, a 3 μm *n*-GaN:Si at 1050℃, 7 pairs of MQWs for each pair with a 3 nm-thick in InGaN well layer and a 7 nm-thick in GaN barrier layer as MQWs at 770~800 ℃, a 50 nm-thick Mg-doped $Al_{0.15}Ga_{0.85}N$ electron blocking layer grown at the temperature of 1000 ℃, and a 0.6 μm *p*-GaN:Mg layer at 1000℃ were grown by metal-organic chemical vapor deposition

(MOCVD) on the c-axis sapphire substrate. Afterward, the mesa area was defined by photolithography to serve as the wet etching mask. The SiO_2 film acted as a CBL, which was grown upon the *p*-GaN:Mg layer via PECVD grown at 180℃ and 280℃ using silane/nitrogen (SiH_4/N_2) mixture as process gas and N_2O gas as carry gas. SiH_4 and N_2O were used to as precursor source for silicon and oxygen. The SiO_2 film was prepared at a lower temperature of 180℃ (hereinafter referred to as LT-CBL SiO_2) and a higher temperature of 280℃ (hereinafter referred to as HT-CBL SiO_2). Then the ITO was deposited utilizing sputter, after that the SiO_2/ITO structure was treated with anneal alloy by rapid thermal annealing (RTA) at 530℃ in nitrogen atmosphere for 1 min. The Cr/Au (30 nm/50 nm) layer was deposited onto exposed n-GaN and ITO, respectively, as the *n*- and *p*-contact.

The surface roughness and morphologies were determined via atomic force microscope (AFM, Veeco Dimension 3100) and scanning electron microscopy (SEM, JEOL JSM-6700P). The average surface roughness of topographical was calculated on an area of 1 μm x 1 μm. Angle resolved x-ray photoelectron spectroscopy (XPS, PHI Quantera SXM) was used to measure the quantitative analysis and determine the N content in the SiO_2:N layer and analyze the chemical bonding state. The reference binding energy position was regulated by Au $4f_{7/2}$ line at 84 eV. All the electrical properties of InGaN/GaN-based LEDs were measured at room temperature. The light output power and far-field radiation patterns were measured using the integrated sphere and a closed black-box with a calibrated power meter.

3. Results and Discussion

The panels (a), (b), and (c) in Fig. 2 show the core level spectra of Si $2p_{3/2}$, O 1s and N 1s of LT-CBL SiO_2, respectively. Si $2p_{3/2}$ and O 1s located at 103.61 and 532.84 eV, but not absorbed any peaks corresponding to N 1s. According to the report by Chen *et al.* [20], the Si $2p_{3/2}$ peak around 103.61eV indicates Si^{4+} in SiO_2. In addition, the core levels of Si $2p_{3/2}$, O 1s, and N 1s of HT-CBL SiO_2 are shown in Figs. 2 (d), (e) and (f), which indicate at 103.95, 533.19, and 399.04 eV, respectively. A quantitative analysis on the XPS spectra determined the atomic composition of N is 2%, meaning the stoichiometric as $SiO_{1.98}N_{0.02}$ in the HT-CBL SiO_2. N 1s peak at 399.04 eV in HT-CBL SiO_2, associating with the nitrogen was replaced by oxygen atoms and the appearance of nitrogen related bonding such as Si-O-N [21-23], but different from the original N 1s locating at 398 eV. As compare with Si 2p core-level and O 1s spectra, the Si 2p and O 1s peak both shifts towards higher binding energy from LT-CBL SiO_2 to HT-CBL SiO_2. The results can be attributed to nitrogen doping into HT-CBL SiO_2, leading to the replacement of partial O sites by N. A stronger electronegativity of oxygen than nitrogen with the Si atom, it might imply that the Si 2p and O 1s spectra shift toward higher binding energy. The results also suggested the partial incorporation of nitrogen in SiO_2 and a dense quality from SEM analysis are caused by the N_2O dissociated at the growth temperature of 280°C.

Figures 3(a) and (b) illustrate a sketch map of the side-wall profile of LT- and HT-CBL SiO_2 during the wet etching process. The buffered oxide etchant (BOE), as wet etching solution, is a mixture of a buffering agent, such as ammonium fluoride (NH_4F) and hydrofluoric acid (HF). The overall chemical reaction involved is normally understood as [24,25]

$$SiO_2 + 6HF \rightarrow 2H^+ + SiF_6^{2-} + 2H_2O \quad (1)$$

Firstly, the silicon oxide can be formatted to Si(-OH)$_x$ in the BOE etching solution. The Si(-OH)$_x$ will react with the different rate constants, such as HF_2^- and HF in the wet etching solution. Shortly afterwards, the SiO_2 would be etched to form SiF_6^{2-}, and then the Si would be taken off. Figures 3(c) and (d) demonstrate SEM image from vertical to cross section of the CBL side-wall profile after 15 sec etching in BOE solution. As compared with HT-CBL SiO_2, the SEM image presents a larger angle (θ) on side-wall profile of LT-CBL SiO_2. Since the LT-CBL SiO_2 has rough surface and less dense structure, the BOE solution easily reacts and passes down through LT-CBL SiO_2 in vertical direction, thus causes the larger side-wall angle of 80˚ (θ_1). In the other words, the etching process of LT-CBL SiO_2 includes faster vertical etching rate and slower horizontal etching rate owing to the incorporation of its less dense structure and rough surface. As for side-wall profile of HT-CBL SiO_2, a dense film quality deserves an isotropic etching in all direction and results in a smaller side-wall angle of 40˚ (θ_2). The result is also corresponding to the SEM cross section image as shown in Fig. 3(d).

To further monitor the side-wall profile of CBL SiO_2, we conducted a simple approach to confirm the profile for each process. The SEM top view of pad and CBL SiO_2 can be corresponding with the cross section structure, as shown in Figs. 4(a) and (b). The lateral distance from point A to B can be measured by SEM as x. The thickness of CBL SiO_2 is in an automatically updated record from PECVD equipment status. Thus the side-wall angle of CBL SiO_2 could be calculated from x and y and the side-wall angle has been determined to be 40˚. The inset in Fig. 4(a) shows the optimal step coverage with a side-wall angle of 40˚ when subsequently grown the sputter-deposited ITO onto HT-CBL SiO_2. As a result, the side-wall profile of HT-CBL SiO_2 can be fine tune under the condition of growth temperature and etching-steps to approach smoothly and flatly for quality electrical device.

Figure 5 shows the normalized power degradation under accelerated reliability test for LT-CBL and HT-CBL LED. The accelerated reliability performance is measured in the high- temperature and humidity (85℃/85 RH) using an injection current of 120 mA for 1000 hours. The degradation of output power in LT-CBL LED is as high as 6.8% during 1000 hours. The results can be attributed to the low temperature grown CBL would form a larger side-wall angle via BOE wet etching. As shown in Fig. 3(c), the vertical strike and rough side-wall of LT-CBL might result in the non-uniform ITO layer grown upon CBL. The thickness of ITO covering on CBL is thinner on vertical direction of side-wall than horizontal direction. A thinner ITO film area has a higher sheet resistance [26], which leads to a large heat accumulated effect while device operation. Thus, the side-wall ITO will crack and the current spreading effect is suppressed, causing drastic power degradation when LT-CBL LEDs operates under the accelerated reliability test. On the contrary, HT-CBL SiO_2 has dense quality and smooth surface as well as a good current blocking layer to resist electron transporting through the *p*-pad and *p*-finger region. It avoids combination of electron and hole in MQWs under the *p*-pad and *p*-finger region. On the other hand, it also means the LEDs with a HT-CBL SiO_2 inserted beneath the *p*-pad electrode and *p*-finger might increase the light-output power, attributing to a reduction in parasitic optical absorption in the *p*-pad electrode and *p*-finger [27-29]. Accordingly, the deposition mechanism of PECVD SiO_2 growth is related an effective surface diffusion length (λ) dependence of diffusion constant (D) [30]. Thus, an increasing in growth temperature would increase diffusion constant and cause the atomic with longer effective surface diffusion length. It suggests that HT-CBL SiO_2 demonstrates the dense quality to be a stable CBL. The HT-CBL SiO_2 will result in optimal step coverage of ITO layer for current spreading and lead to the HT-CBL LEDs degrade as low as 5% in the accelerated reliability test.

4. Conclusion

In summary, the side-wall profile of HT-CBL SiO_2 has been optimized to fabricate InGaN/GaN-based LEDs. The HT-CBL SiO_2 shows dense structure quality and smooth surface than the LT-CBL SiO_2. The HT-CBL SiO_2 reduces the parasitic optical absorption under the *p*-pad electrode and *p*-finger, thus obtaining small side-wall angle of CBL and forming good step coverage while ITO is deposited upon CBL. The analysis of XPS spectra suggests the partial incorporation of nitrogen into HT-CBL SiO_2 and a dense quality from SEM analysis are caused by the N_2O dissociated at the growth temperature of 280℃ via the plasma process in PECVD technique. An approach via SEM cross section analysis and thickness of CBL is conducted to confirm the profile of side-wall. The HT-CBL SiO_2 shows a small side-wall angle of 40˚ which increases the step coverage and current spreading of ITO. The HT-CBL LED demonstrates a good performance in high injection current, since HT-CBL effectively suppresses current directly pass through from pad to GaN. Consequently, the HT-CBL SiO_2

exhibits optimal step coverage of ITO film for current spreading and then the HT-CBL LEDs demonstrate superior reliability under the accelerated reliability test. The results indicate it is feasible for high-power device application.

Acknowledgements

This work was financially supported by the EPISTAR Corporation. The authors would also like to thank the National Science Council of the Republic of China, for financially supporting this research under Contract No. MOST105-2221-E-214-018-MY3 and 108-2221-E-214-027.

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FIGURE CAPTIONS

Fig. 1. Schematic diagram of LED structure.

Fig. 2. The XPS spectra for Si $2p_{3/2}$, O 1s and N 1s of the LT-CBL and HT-CBL SiO_2, respectively.

Fig. 3. A sketch map for wet etching process of (a) LT-CBL and (b) HT-CBL SiO_2 side-wall profile. The SEM image from vertical to the cross-section of side-wall profile of (c) LT-CBL and (d) HT-CBL SiO_2 after etching in BOE solution.

Fig. 4. (a) The SEM top view of pad and CBL SiO_2. The inset is the SEM cross-section of the side-wall HT-CBL SiO_2. (b) A simple approach to confirm the CBL SiO_2 side-wall profile.

Fig. 5. The normalized power degradation under accelerated reliability test for LT-CBL and HT-CBL LED in the high-temperature and humidity (85°C/85 RH) using an injection current of 120 mA for 1000 hours.

Figure 1

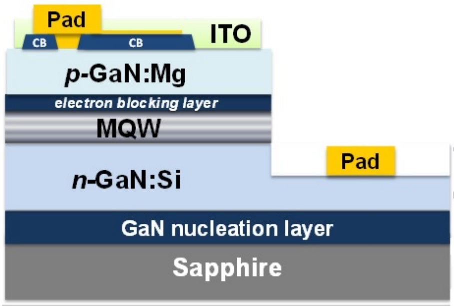

Pad
CB
CB
ITO
p-GaN:Mg
electron blocking layer
MQW
Pad
n-GaN:Si
GaN nucleation layer
Sapphire

Figure 2

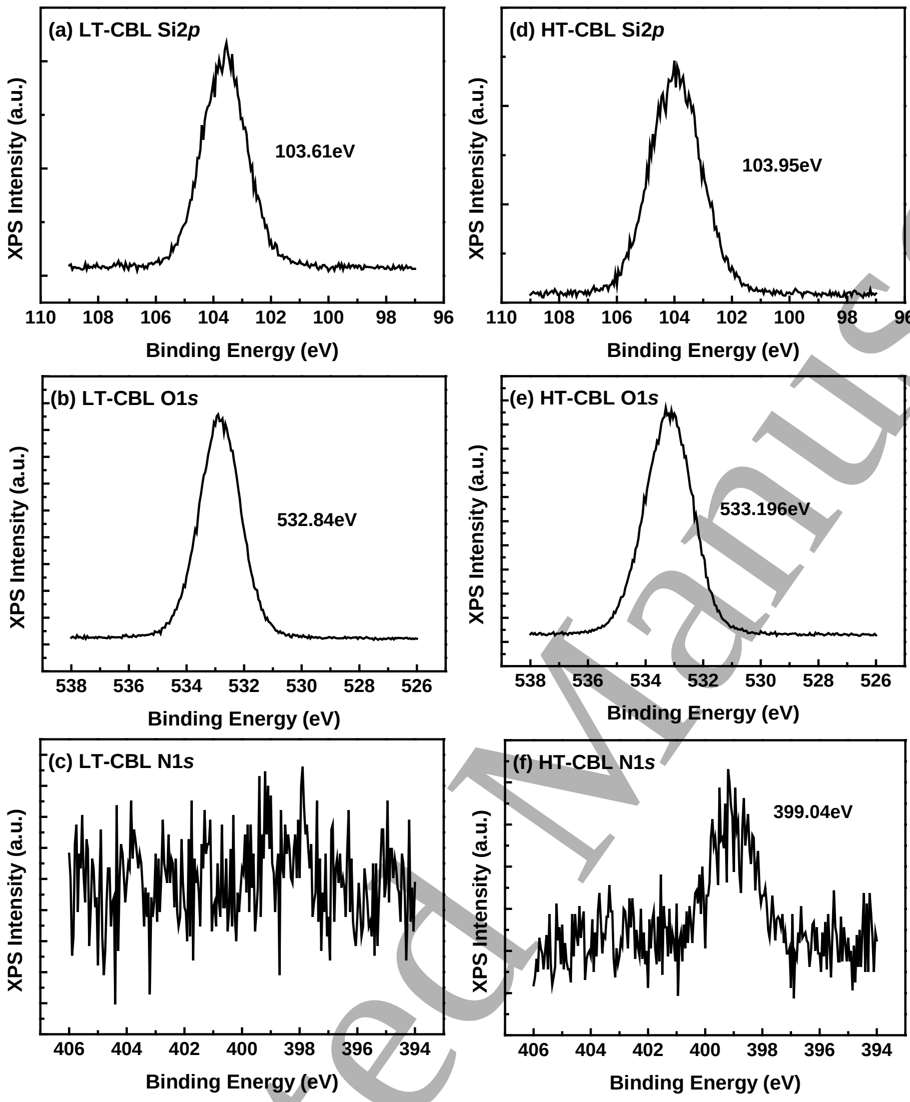

(a) LT-CBL Si2p
103.61eV
(b) LT-CBL O1s
532.84eV
(c) LT-CBL N1s
(d) HT-CBL Si2p
103.95eV
(e) HT-CBL O1s
533.196eV
(f) HT-CBL N1s
399.04eV
XPS Intensity (a.u.)
Binding Energy (eV)

Figure 3

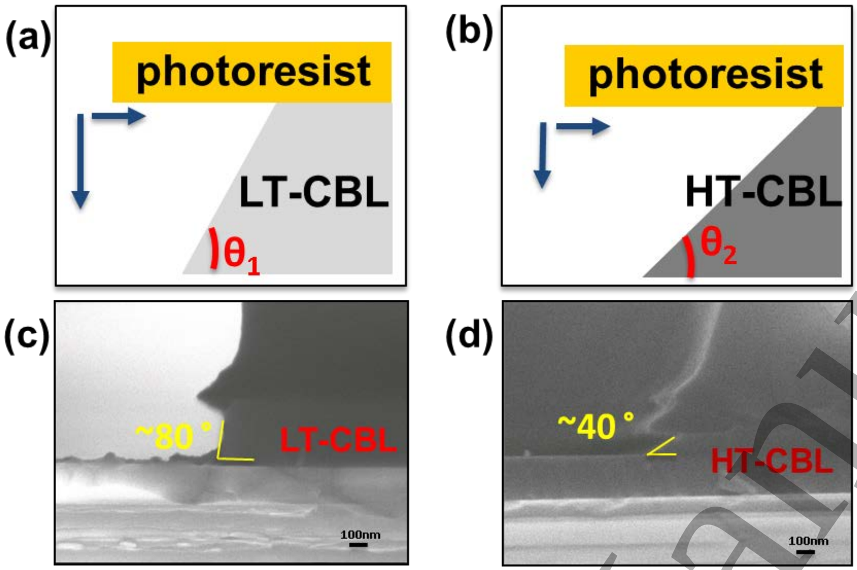

(a)
photoresist
LT-CBL
θ1
(b)
photoresist
HT-CBL
θ2
(c)
~80 °
LT-CBL
100nm
(d)
~40 °
HT-CBL
100nm

Figure 4

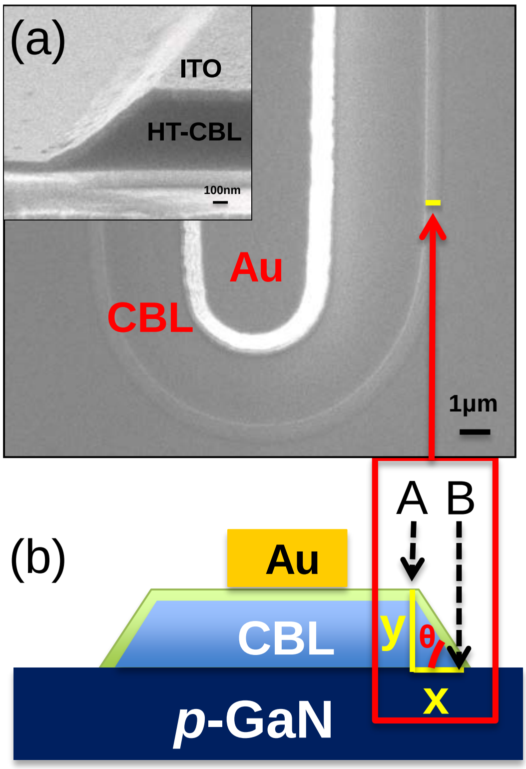
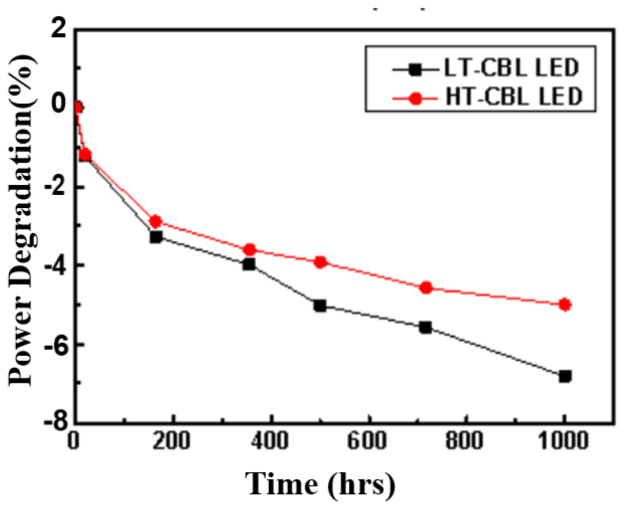


Figure 5.



Power Degradation(%)
Time (hrs)
LT-CBL LED
HT-CBL LED
2
0
-2
-4
-6
-8
0
200
400
600
800
1000