

Advanced Manufacturing Techniques for Next Generation power FET Technology

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Abstract - The development and incorporation of an evaporated airbridge technology into an established power pHEMT device is described. Advantages of this technology over a conventional plated technology are discussed. Use of this technology has resulted in improvements to the process flow in terms of reduced complexity and cycle time. Improvements in uniformity and reduced feature size have enabled the use of an automated visual inspection capability to reliably differentiate good and bad die.

I. INTRODUCTION

Base station power amplifier modules are seen as a key product for Filtronic PLC. During the past 24 months, Filtronic Compound Semiconductors has invested heavily in developing a power FET process in order to supply an in house source of GaAs pHEMT die.

Development of the power FET process route has produced a robust, manufacturable technology capable of delivering high yields and device performance [1, 2]. Typically, product die exhibit 0.5 W /mm output power for large periphery die operating at 2GHz from a 12 volt supply voltage.

In addition to demonstrating very high product DC / RF yields, a further requirement prior to shipping to customers is an end of line visual inspection to satisfy defect levels and confirm the cosmetic quality of the die. The visual appearance of the current gold plated metalization used for metal interconnects and airbridge technology on this process route has made it challenging for automated inspection tools to distinguish gold pad surface roughness from defects at sub micron level. The effect this can have is dramatic as manual visual inspection is required which is very labour intensive, increasing fab cycle times and enhancing cost efficiency. In addition, manual visual inspection may potentially introduce variation in inspection quality, thus compromising the reliability and repeatability of the visual data.

An alternative to the gold plated airbridge process has been developed utilising existing toolsets within the facility to produce an evaporated metal process capable of depositing $> 4\mu\text{m}$ of metalization [3]. In addition to the improved visual appearance of the evaporated metalization, a number of additional advantages have been gained by the use of this technology.

- Improved linewidth control
- Reduced pattern distortion
- Improved thickness uniformity
- Reduced cycle time
- Reduced processing steps

This paper reviews the techniques utilised to create this technology and dicusses some of the challenges faced in implementing the technology into a production environment.

II. PROCESS DEVELOPMENT

The construction of a conventional gold plated airbridge requires a combination of process steps from different process areas. A typical process flow would involve the following steps:

- Airbridge foot photolithography to define bridge span
- Sputtered metal seed deposition
- Airbridge photolithography
- Airbridge gold plating
- Resist strip
- Metal seed etchback
- Footing resist strip

Although the basic concept is straightforward, there are a number of variations and complexities which have to be taken into account during the process set up. For example, the footing resist layer must be baked sufficiently to withstand the sputtered seed layer metalization, but must not be overbaked or it will be difficult to remove from beneath the plated airbridge. The airbridge resist layer must be sufficiently baked to withstand the plating environment, which in turn may also affect the final profile of the plated metalization. Gold plating rate is also highly dependant on pattern density. All these factors add to the complexity of process development [4]. A typical gold plated airbridge structure is shown in Figure 1.

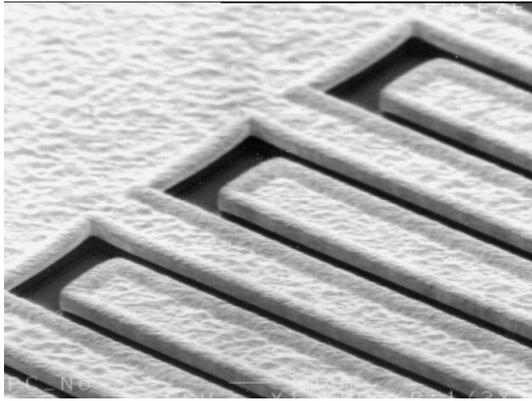


Figure 1: Gold plated airbridge

The development of an evaporated airbridge structure reduces the complexity of the process. The main process steps required to produce the structure are:

- Bridge photolithography to define bridge span
- Airbridge photolithography
- Airbridge deposition
- Lift off/ resist strip

The first step is to perform the bridge photolithography to define the bridge shape. A conventional i-line photoresist is used and spun to a thickness of approximately $3\mu\text{m}$. Exposure is carried out using a Nikon NSR 2205 i11C Step and Repeat system. Following resist develop, a reflow bake is then performed to stabilize the resist, and to round the resist profile aiding the subsequent step coverage of the evaporated metalization.

The second stage is the definition of the airbridge structure. For this step, a negative tone photoresist has been adopted. Careful optimization of the softbake, exposure conditions and post exposure bake have resulted in a profile tailored for lift off of an evaporated metalization. Resist thicknesses of the order of $6\mu\text{m}$ have been adopted. Exposure is carried out using a Nikon NSR 2205 i11C Step and Repeat system

Following airbridge lithography, metal deposition is carried out using a Ti/Pt/Au metalization. A Temescal FCE 2700 e-beam evaporation system has been utilised for this step. Metalization thicknesses in excess of $4\mu\text{m}$ have been demonstrated. Figure 2 shows a cross sectional image of an evaporated metal structure prior to lift off processing. The re-entrant slope achieved by the use of a negative tone resist is evident, providing an excellent means for a lift off process. Good edge definition is achieved from the evaporation process.

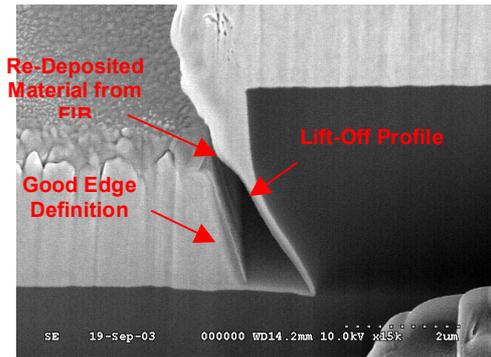


Figure 2: Cross sectional image of evaporated metal pre lift off.

The final stage of the process is to lift off the unwanted evaporated metalization leaving the intact airbridge in place. An automated solvent spray system has been optimized to lift off the metal and remove the photoresist. An oxygen plasma ash completes the clean up process. Figure 3 shows a typical evaporated airbridge structure.

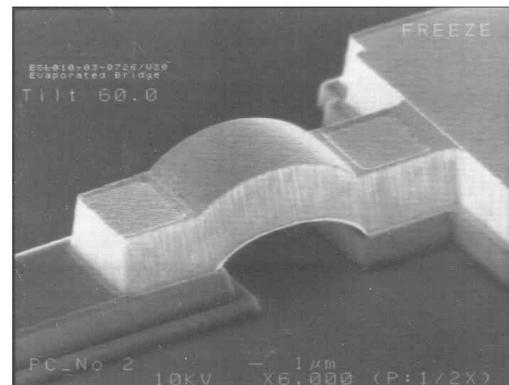


Figure 3: Evaporated airbridge structure

A large gate periphery power FET device (180mm) utilizing this evaporated airbridge technology is shown in Figure 4

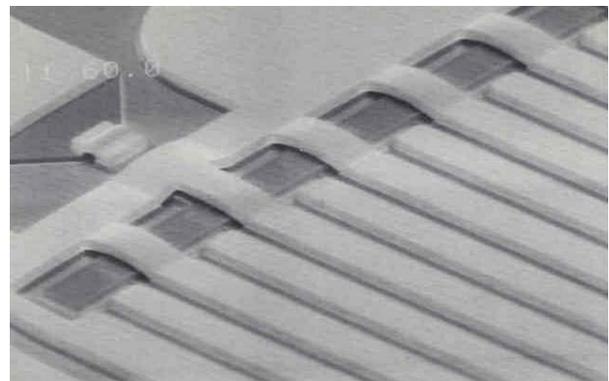


Figure 4: Large gate periphery power FET utilizing evaporated airbridge technology.

III. VISUAL INSPECTION

Automated visual inspection has been carried out using an August Technology NSX 85 defect inspection tool. Inspection is carried out at the end of the fabrication cycle. Wafers are thinned to between 50-150 μm depending on the product application. The thinned wafers are mounted onto a film frame and the film frame is manually loaded into the inspection tool.

Typical defects picked up by an inspection tool would be, for example: scratches, contamination, particles, metal shorts, metal opens, metal frills. It is critical that the defect sensitivity and inspection criteria are defined clearly within the operating recipe to ensure adequate throughput is maintained. Following inspection, electronic wafer maps are available to allow defect classification to take place. Defects would normally be classified to provide a pareto analysis to highlight problematic areas. Defects could then be correlated against known DC / RF fails from electrical test. Implementing this automated inspection process into a mass production environment also requires creation of appropriate working procedures and operational documentation, as well as the training of fab personnel.

Utilising this automated system, inspection times of 5 mins per wafer, equating to a throughput of 12 wafers per hour have been sampled. When compared to manual inspection, cycle time has been improved by a factor of 4. Optimization of the program recipes by assigning appropriate pass / fail criteria to filter out non-process related defects will further enhance inspection quality.

Figure 5-6 illustrates the differences observed in surface morphology between an evaporated metal structure and a gold plated structure.

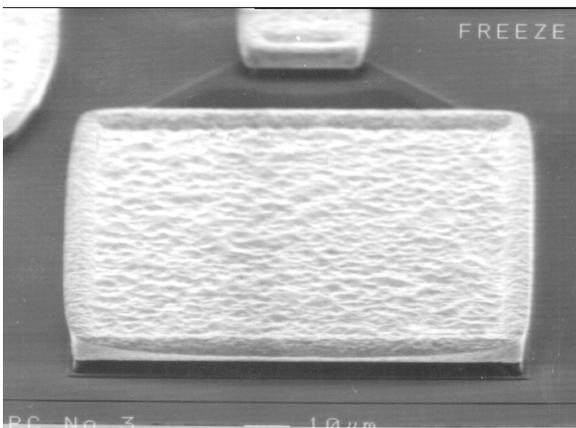


Figure 5: Typical Gold plated surface morphology

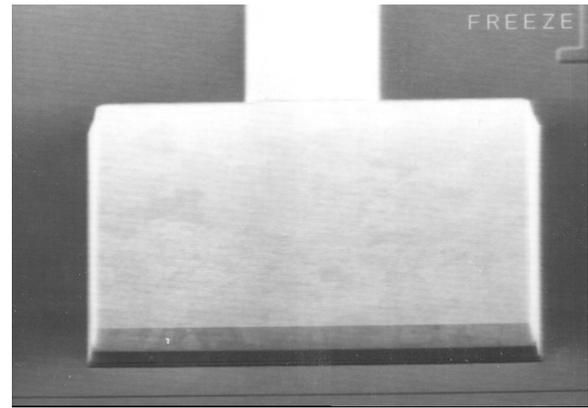


Figure 6: Typical Evaporated gold surface morphology

A typical wafer map generated by the August inspection tool is shown in Figure 6. Dark areas indicate a defect requiring classification.

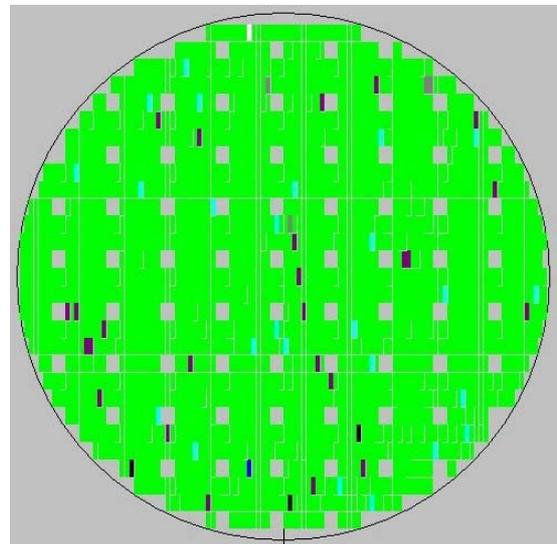


Figure 6: Typical defect wafer map generated by August inspection tool

IV. CONCLUSIONS

An evaporated airbridge technology has been demonstrated and incorporated into an established power FET production process. Adopting this approach over a conventional gold plating technology traditionally used has enabled the use of an automated visual inspection system to be utilized at end of line, providing improved fabrication cycle times. In addition to this, use of this technology also offers a number of process enhancements, for example: improved linewidth control, improved thickness uniformity, reduction in pattern distortion and reduction in process complexity.

ACKNOWLEDGEMENTS

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ACRONYMS

FET:	Field Effect Transistor
PHEMT:	pseudomorphic High Electron Mobility Transistor
FCE:	Fast Cycle Evaporator
NSR:	Step and Repeat exposure system