The 6th ASME-JSME Thermal Engineering Joint Conference
March 16-20, 2003

TED-AJ03-332

INTEGRATED ELECTROPLATED HEAT SPREADERS FOR HIGH POWER SEMICONDUCTOR LASERS

Jianping Fu, Ronggui Yang, Gang Chen
Mechanical Engineering Department, Massachusetts Institute of Technology
Cambridge, MA 02139, USA
Email: gchen2@mit.edu

Jean Pierre Fleurial, G. Jeffrey Snyder
Jet Propulsion Laboratory, 4800 Oak Grove Drive
Pasadena, CA 91109, USA

Keywords: Heat Spreader; Semiconductor Laser; Thermal Management; MEMS

ABSTRACT

Thermal management of high power semiconductor lasers and laser arrays is demanding and challenging due to the low thermal conductivity of the laser substrate and active device layers. In this work, metal heat spreaders of high thermal conductivity directly electroplated on the semiconductor lasers is investigated to improve the laser performance by avoiding the use of low thermal conductivity interface materials and thus reduce the thermal resistance of the lasers. Copper heat spreaders with different sizes are directly electroplated on the structures that mimic edge-emitting semiconductor lasers. The size effect of these heat spreaders is experimentally demonstrated through comparison with reference samples. A two-dimensional analytical model is developed to verify the thermal resistance experimental data. The results from the model fit the experimental data very well.

NOMENCLATURE

K	thermal conductivity ($W/m^2 \cdot K$)
R	thermal resistance (K/W)
Q	heat (W)
A	area (m^2)
W	width (m)
L	length (m)
T	thickness (m)
B	series constant

SUBSCRIPTS

1	heat going down
2	heat going up
n	natural number
s	substrate
h	heater
in	insulator
sp	heat spreader
heater	metallic heater region
heating	metallic heating area

INTRODUCTION

High power semiconductor lasers have found broad applications in solid-state laser pumping, direct materials processing, medical surgery, printing and manufacturing [1,2]. The maximum optical output power of semiconductor lasers, however, is limited by the temperature rise in the active region [3,4]. The self-heating of the lasers also causes other effects that degrade laser performance, such as wavelength shift, changes of the mode and beam profile, and shortened lifetime. The thermal management of high power semiconductor lasers and laser arrays is especially challenging due to the low thermal conductivity of their substrates and the functional layers used in these lasers [5,6].

The thermal characteristics and thermal management of semiconductor lasers have been investigated by various researchers [7-14]. Most of these works in thermal management use the configuration of junction-side-down mounting to spread the heat out, either passively through high thermal conductivity substrates [7-11, 13] or actively through integrated microchannel cooling systems [12, 14]. The laser is bonded to the heat spreader through relatively low thermal conductivity solder materials, which can limit the performance of the laser [7, 13].

In this work, the use of copper heat spreaders directly plated on top of the laser is proposed to reduce the thermal resistance between the active heating region of the laser and the external cooling system. With its high thermal conductivity, an electrochemically plated copper heat spreader eliminates the use of the low thermal conductivity interface materials between the laser bar and the heat spreader, thus avoiding the bonding process and the interface imperfections generated in the soldering process. For example, voids in the soldering layer have been found to give rise to hot spots and therefore increase the thermal resistance [8].

To investigate the effectiveness of the directly plated heat spreaders, test structures modeling the thermal characteristics of high power semiconductor lasers are

fabricated with integrated metallic heaters and temperature sensors. The thermal resistances of the test samples are measured with junction-side-up mounting configuration, which is more effectively improved by the heat spreader structure [13]. A two-dimensional analytical model is developed to verify the thermal resistance experimental data of the test samples.

DESIGN AND FABRICATION

We aim at mimicking edge emitting laser structures [15], including high-power quantum-well edge-emitting lasers and quantum cascade lasers [16]. In the quantum-well based edge-emitting lasers, cladding layers are used to confine the carriers and the light. These cladding layers are typically made of alloys that have low thermal conductivity. Heat is generated both in the cladding layers by resistive heating and in the active region by the nonradiative recombination. In quantum cascade lasers, thick superlattice structures are used as the lasing region, which experiences both resistive heating and nonradiative recombination heating. The superlattice structures have even lower thermal conductivity than their equivalent alloys, leading to more severe heating problems in quantum cascade lasers [17].

As shown in Fig. 1, a test structure is designed in this work to model the thermal characteristics of semiconductor lasers and also test the effectiveness of the integrated plated copper heat spreaders. In such a design, a meander-shaped heater stripe is embedded between two dielectric layers that have low thermal conductivity. By controlling the thickness of the dielectric layers, their thermal resistance can be matched to that of actual laser device layers. The heater also serves as a resistive thermometer to measure the temperature rise under different heating power conditions.

Figure 2 shows the fabrication process flow of the electroplated copper heat spreader structure. A GaAs wafer is chosen as the substrate because many semiconductor lasers are built on this material. Other substrate materials for semiconductor lasers, such as GaSb, have similar thermal properties. Test samples with

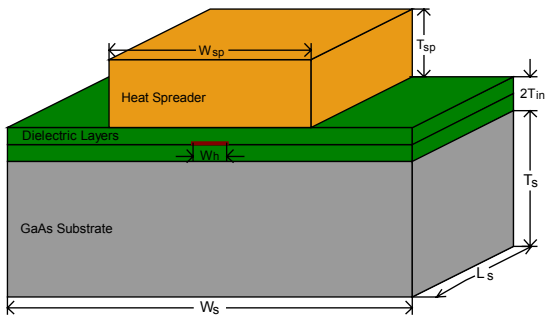

Figure 1, Schematic illustration of the test structure used for evaluating the effectiveness of the integrated heat spreaders for high power semiconductor lasers. The meander-shaped microheater stripe is embedded between two dielectric layers. High thermal conductivity copper is deposited on top of the structure to serve as heat spreader.

Si as substrate also are fabricated in the same way for comparison. After the initial cleaning steps, a one-micron thick dielectric layer (silicon nitride or silicon dioxide) is deposited by a plasma enhanced chemical vapor deposition (PECVD) method in multiple steps. This 1μm dielectric layer serves to mimic the low thermal conductivity device layers in semiconductor lasers with comparable thermal resistance. The multi-deposition of dielectric layers is needed to reduce the number of pinholes and thus ensure the metallization test pattern is electrically insulated from the substrate [18]. Since our experimental measurement makes use of the linear temperature-resistance relation of the metallic heater, any current leakage between the test pattern and the substrate can easily ruin the measurement.

After the first dielectric layer deposition, the first photolithography step is performed to define the metallic heaters. A multilayer (Ti/Pt/Au/Ti=200Å/300Å/1500Å/200Å) is deposited by electron-beam evaporation and followed by lift-off to form the heaters. The first thin titanium layer is an adhesion layer for gold to the underlying dielectric layer. The platinum layer serves as a diffusion barrier to gold. The topmost titanium layer is intended to improve the adhesion of the top PECVD dielectric layer to be deposited later. After the lift-off process, another 1μm PECVD dielectric layer is deposited as an insulation layer. This layer also serves to mimic the top cladding or superlattice layers in real semiconductor lasers. Another photolithography step is then performed to open electrical contact pads through the second dielectric layer by reactive ion etching (RIE). After the opening of electrical contact pads, a seed layer (Ti/Cu/Ti=300Å/6000Å/300Å) for future copper plating is deposited by electron-beam evaporation. The copper seed layer is of sufficient thickness to ensure uniform plating across the entire 2-inch wafer with minimal resistivity effects. The first titanium layer is an adhesion layer of copper for the underlying dielectric layer, and the second serves as adhesion layer for the thick photoresist to be spun-on later. The top layer of titanium is also used to prevent oxidation of the copper seed film during subsequent processing steps leading up to copper electroplating.

After the seed layer deposition, negative thick photoresist NR9-8000, from Futurrex, Inc., is applied to achieve thick plating molds. Photoresist molds thicker than 100μm have been obtained with single spin and double spin methods [19]. After development with Futurrex RD6 developer, the thick NR9-8000 mold can be optionally thermally cured to achieve increased resistance to chemical attack. However this cure results in the distortion/shrinkage of the pattern, which substantially decreases the height of the film as well as compromise the sharpness of the sidewalls. The structures described in this work use a NR9-8000 mold that is not thermally cured prior to electroplating; the detailed trade-off between photoresist cure and feature distortion/shrinkage is not examined in this work.

After patterning the photoresist mold, the topmost titanium layer is removed by a quick dipping into dilute

buffered-oxide-etchant (BOE) to expose the thick copper seed layer. After a deionized water rinse of the samples, a short ultrasonic treatment in deionized water is needed to remove the entrapped air and to ensure intimate contact between the solution and the seed layer during plating.

Copper electroplating is performed using a commercially available acid copper plating solution (Technic Copper RTU-type). The size of the copper anode is designed to be about 5cm by 5cm, so that the ratio of the anode to cathode area is about 1:1. At the beginning of the electroplating, the DC current is set to a low value and increased stepwise slowly, in order to ensure uniform copper plating. The slow current ramping also ensures that the wetting agent in the bath adheres to the top of cathode to provide good surface wetting, which aids in bubble prevention. Stresses in the plated copper are also minimized by starting with small plating current [20]. The plating current density is limited to 20mA/cm^2, yielding an approximate deposition rate of 0.4-0.5μm/min. It takes about three hours to plate an 80μm thick copper in the mold. After plating is complete, the NR9-8000 photoresist mold is completely removed in an acetone bath.

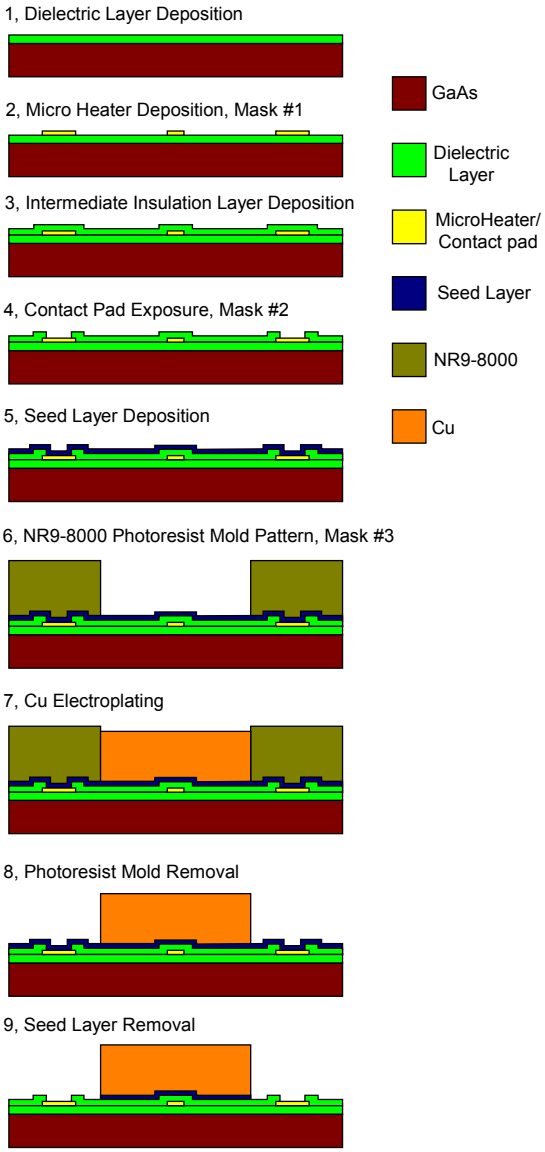

Figure 2, Fabrication process flow of the integrated copper heat spreader structure.

Electrical isolation of the electroplated heat spreaders is achieved by etching away the seed layers. A brief dip in dilute BOE is performed to remove the two titanium layers separately. A dilute nitric acid bath together with citric acid ($C_6H_8O_7 \cdot H_2O$) is used to remove the copper seed layer. The citric acid is believed to reduce the etch rate of copper in nitric acid and to reduce the non-uniformity of the finished copper surface [21].

After dicing the wafers into small individual samples they are ready for testing.

EXPERIMENTAL DATA

Experiments are performed with two kinds of test samples, one with copper heat spreaders (as shown in Fig. 2, step 9, “device sample”) and another without, but all other structure layers are identical (Fig. 2, step 4, “reference sample”). The latter serves as a reference to gauge the effectiveness of the plated copper heat spreader. The measurements are divided into two steps. The first step is to characterize the temperature coefficient of resistance (TCR) of each sample under a low current loading. The second step is to measure thermal resistances of the samples under the junction-side-up mounting configuration.

Before experiments, all the samples are junction-side-up mounted on a copper heat sink (4” diameter, 1” thickness) with a thin thermal grease layer. A fine type-K thermocouple is attached in close proximity to the sample on top of the copper sink. This type-K thermocouple is used to determine heater temperature during the TCR calibration and also to measure the temperature at the sample bottom surface during thermal resistance measurement.

TCR of all the samples are calibrated by measuring electrical resistances of the metallic heaters using the four-probe method while they are heated in an isothermal environment to different temperatures. The thermal resistance measurement is performed by passing a current through the heater. The metallic heater is heated electrically and its resistance increases with the increasing temperature. The resistance and heating power is determined by measuring the current and voltage drop across the heater from the four leads. Knowing the TCR from the first measurement step, the heater temperature can be determined from its resistance. The temperature of the sample bottom surface is measured at the same time by the type-K thermocouple. The thermal resistance of the heat spreader test sample is then determined. Figure 3 shows a typical set of such experimental data. The numbers indicated in the figure are scaling factors that are defined as the ratio of the heat spreader width divided by the metallic heater width. Slopes of the curves give thermal resistances of the test samples, defined as $\Delta T / P$.

Figure 4 shows the thermal resistance experimental data of GaAs samples with heat spreaders of different

widths. The heater area of GaAs samples is 750μm×120μm and the thickness of the copper heat spreaders is about 80μm. Test samples with Si as substrate are also fabricated and tested. Figure 5 shows thermal resistance data of Si samples with heat spreaders of different widths. The heater area of these samples is 360μm×100μm and the thickness of the heat spreaders is also about 80μm. The dielectric layers used in Si samples are PECVD silicon dioxide, which is different from silicon nitride layer deposited on GaAs samples. The silicon dioxide is found to work better as an insulator layer. In both figures, the reference sample data is included for comparison.

As seen from Fig. 4 and Fig. 5, the thermal resistances of the device samples are strongly reduced by the top plated copper heat spreader. Most of the heat generated in the heater region flows up to the plated copper layer, spreads out, and then flows down through the test structure over a large area. Most of the benefit comes from the first few scaling factors. With a heat spreader scaling factor of 5, the thermal resistances of both GaAs and Si test samples reduce about 50% with junction-side-up mounting configuration.

MODELING

A two-dimensional analytical model to calculate the thermal resistance of the test structure is developed in this work. In this model (as shown in Fig. 6), no heat escapes through the sides, ends, or top of the test structure. The bottom of the substrate is maintained at a constant temperature. Heat (Q) is generated uniformly and steadily in the planar meander-shaped heater. Part of the heat (Q_1) goes down directly through the bottom dielectric layer and the substrate into the heat sink; the rest ($Q_2 = Q - Q_1$) enters the copper heat spreader through the top dielectric layer and spread laterally. This part of heat re-enters the

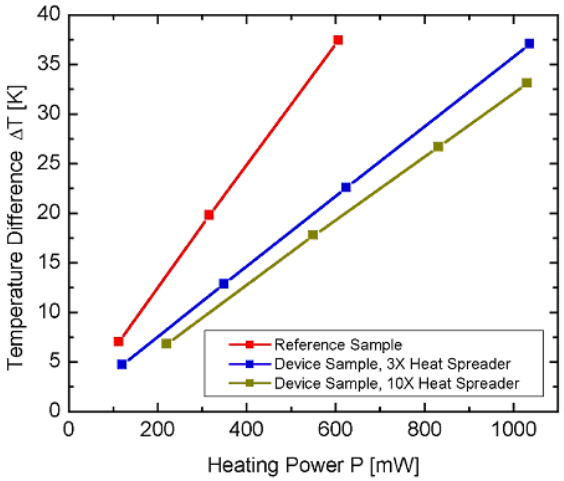

Figure 3, Temperature difference ΔT between heaters and sample bottom surfaces as a function of heating power P. Experimental data are from Si samples with SiO_2 as dielectric layers (heater: 360μm×100μm; copper heat spreaders thickness: 80μm).

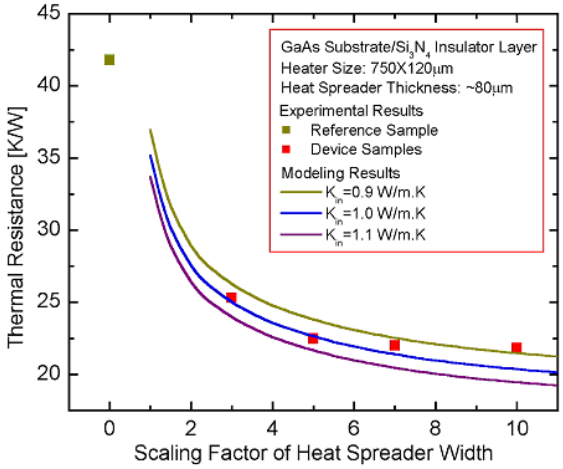

Figure 4, Experimental data of the thermal resistances of GaAs samples with different heat spreader widths. Reference sample is included for comparison. Three curves from analytic modeling are also plotted. Different thermal conductivity values of Si_3N_4 are used to fit the experimental data.

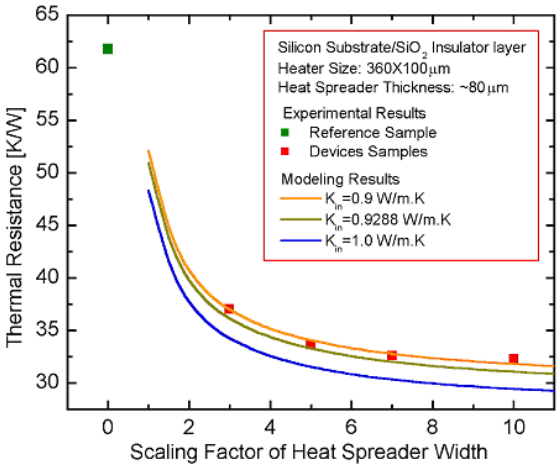

Figure 5, Experimental data of the thermal resistances of Si samples with different heat spreader widths. Reference sample is included for comparison. Three curves from analytic modeling are also plotted. Different thermal conductivity values of SiO_2 are used to fit the experimental data. $K_{in} = 0.9288 W/m \cdot K$ is determined by fitting the thermal resistance of the reference sample with the analytical model result.

dielectric layers and substrate, and finally flows into the heat sink. For Q_1, heat flow is assumed to be one-dimensional in the bottom dielectric layer and the corresponding thermal resistance $R_{in-bottom}$ is given by $R_{in-bottom} = \dfrac{T_{in}}{K_{in} \cdot A_{heating}}$; the two-dimensional heat flow of Q_1 in the substrate will have thermal resistance of R_1. For Q_2, heat flow is one-dimensional in the top dielectric layer and the corresponding thermal resistance is R_{in-top}. R_{in-top} is given by $R_{in-top} = \dfrac{T_{in}}{K_{in} \cdot A_{heating}}$ also, for the

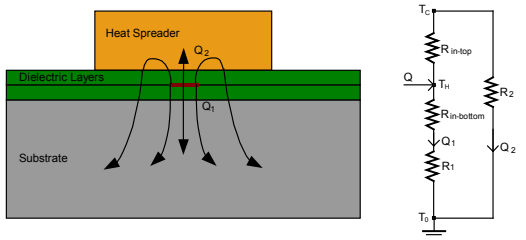

Figure 6, Two-dimensional analytical model for the test heat spreader structure. Left: two-dimensional structure picture of the test sample; right: thermal circuit for the calculation of the thermal resistance of the test sample.

two dielectric layers have the same thickness; thermal resistance from the top heat spreader layer to the substrate bottom is calculated as R_2. The two dielectric layers and the heat spreading effect of the copper heat spreader are included into the top side of the substrate as boundary conditions when calculating R_2.

The thermal resistances R_1, R_2 are calculated from the separation of variable solution of Laplace's equation for two-dimensional rectangular substrate plate with left and right sides adiabatic, and bottom side at a constant temperature [22]. Special care needs to be taken for the inhomogeneous boundary conditions at the top side of the substrate used to calculate the separation constants. The thermal resistances R_1, R_2 are determined as follows:

$$R_1 = \frac{T_s \cdot W_h}{W_s \cdot K_s \cdot A_{heater}} + \frac{1}{K_s A_{heater}} \cdot \sum_{n=1}^{\infty} [-\frac{W_s^2}{(n\pi)^3 \cdot W_h} \cdot \sin^2(\frac{n\pi W_h}{W_s}) \cdot (1 - e^{\frac{4n\pi T_s}{W_s}}) / (1 + e^{\frac{4n\pi T_s}{W_s}})] \quad (1)$$

$$R_2 = \{2K_s \cdot L_h \cdot [\frac{B_0 \cdot W_{sp}}{2} + \sum_{n=1}^{\infty} (-B_n) \cdot (1 + e^{\frac{4n\pi T_s}{W_s}}) \cdot \sin\frac{n\pi W_{sp}}{W_s}]\}^{-1} \quad (2)$$

The unknown separation constants $B_n (n = 0,1,2,3.....)$ in Eq.(2) are calculated from a set of linear equations that are determined from the matching conditions of heat flux at the top side of the substrate. Thus the total thermal resistance of the test structure is determined as:

$$R_{total} = \frac{(R_{in-bottom} + R_1) \cdot (R_{in-top} + R_2)}{(R_{in-bottom} + R_{in-top} + R_1 + R_2)} \quad (3)$$

The modeling results of the thermal resistances of the GaAs and Si test samples are included in Fig.4 and Fig.5. Because the thermal conductivities of the SiO_2 and SiN_x layer are process-dependent and vary with temperature, different values are used to fit the experimental data as indicated in the figures. All the thermal conductivity values used for PECVD SiO_2 and SiN_x are in the reasonable range as reported in the literature [18]. The agreement between the analytical modeling results and the experiment data is very good.

CONCLUSION

Testing structures to model the thermal characteristics of high power semiconductor lasers are fabricated in this work to investigate the effectiveness of the top heat spreader layers. Samples with copper heat spreaders of different widths are tested. Experimental results show that the thermal resistances of junction-side-up mounted semiconductor lasers are improved dramatically by the top plated copper heat spreaders. A two-dimensional thermal analytical model is developed. The experimental results show a very good agreement with the analytical results.

ACKNOWLEDGMENTS

This work is supported by the DARPA HERETIC project through JPL. We would like to thank Professor S. Pei for useful discussions.

REFERENCES

[1]Welch, D.F., "A Brief History of High-Power Semiconductor Lasers," IEEE Journal of Selected Topics In Quantum Electronics, Vol.6, No.6, Nov./Dec. (2000), pp.1470-1477

[2]Diehl, R (ed.), "High-Power Diode Lasers, Fundamentals, Technology, Applications," New York, Springer, 2000

[3]Hasnain, G., Tai, K., Yang, L., Wang, Y.H., Fischer, R.J., Wynn, J.D., Weir, B., Dutta, N.K., and Cho, A.Y., "Performance of Gain-Guided Surface Emitting Lasers With Semiconductor Distributed Bragg Reflectors," IEEE Journal of Quantum Electronics, Vol.27, No.6, June (1991), pp.1377-1385

[4]Scott, J.W., Geels, R.S., Corzine, S.W., and Coldren, L.A., "Modeling Temperature Effects and Spatial Hole Burning to Optimize Vertical-Cavity Surface-Emitting Laser Performance," IEEE Journal of Quantum Electronics, Vol.29, No.5, May (1993), pp.1295-1308

[5] Ueno, Y., Endo, K, Fujii., H., Kobayashi, K., Hara, K., and Yuasa, T., "Continuous-Wave High-Power (75mW) Operation of A Transverse-Mode Stabilised Window Structure 680nm AlGaInP Visible Diode", Electronic Letters, Vol.26 (1990), pp.1726-728

[6]Chen, G., "Heat Transfer in Micro- and Nanoscale Photonic Devices," Annual Review of Heat Transfer, Vol. VII (1996), pp.1-57

[7]Joyce, W.B., and Dixon, R.W., "Thermal Resistance of Heterostructure Lasers," Journal of Applied Physics, Vol.46, No.2, Feb. (1975), pp.855-862

[8]Kobayashi, T. and Iwane, G., "Three Dimensional Thermal Problems of Double-Heterostructure Semiconductor Lasers", Japanese Journal of Applied Physics, Vol.16, No.8, Aug. (1977), pp.1403-1408

[9]Newman, D.H., Bond, D.J., and Stefani, J., "Thermal-Resistance Models for Proton-Isolated Double-Heterostructure Lasers," Solid-State and Electron Devices, Vol.2, No. 2, Mar. (1978), pp.41-46

[10]Kastigar, S.M.S, Hendron, R.E., Lapinski, J.R. and Hertzler, G.R., "Wafer Thin Coolers for Continuous Wave (CW) Aluminum Gallium Arsenide/Gallium Arsenide (AlGaAs/GaAs) Monolithic Linear Diode Laser Arrays,"

Proceedings of SPIE Vol. 1043 (1989), pp.359-367
[11]Nakwaski, W., “Three-Dimensional Analysis of A Heat-Spreading Phenomenon in Phase-Locked Arrays of Oxide-Isolated Diode Lasers,” Journal of Applied Physics, Vol.67, No.6, Mar. (1990), pp.2711-2715
[12]Lin, Y., Fang, Z., “Thermal Characteristics of Semiconductor Laser Phase-Locked Arrays with Diamond Film Heatsink,” Electronic Letters, Vol.27, No.1, Jan. (1991), pp.18-19
[13]Martin, O.J.F., Bona, G.-L. and Wolf P., “Thermal Behavior of Visible AlGaInP-GaInP Ridge Laser Diodes,” IEEE Journal of Quantum Electronics, Vol.28, No.11, Nov. (1992), pp.2582-2588
[14]Beach, B., Benett, W.J., Freitas, B.L., Mundinger, D., Comaskey, B.J., Solarz, R.W., Emanuel, M.A., “Modular Microchannel-Cooled Heat Sink for High Average Power Laser-Diode Array’”, IEEE Journal of Quantum Electronics, Vol.28, No.4, Nov. (1992), pp.966-976
[15]Yariv, A., “Quantum Electronics”, 3rd Ed., New York, Wiley, 1989
[16]Faist, J., Capasso, F., Sivco, D.L., Sirtori, C., Hutchinson, A.L., and Cho, A.Y., “Quantum Cascade Laser,” Science, Vol.264 (1994), pp. 553-556
[17]Chen, G., “Phonon Heat Conduction in Low-Dimensional Structures,” Semiconductors and Semimetals, Vol.71 (2001), pp.203-259
[18]Lee, S.-M., Cahill, D.G., “Heat Transport in the Dielectric Films,” Journal of Applied Physics, Vol.81, No.6, Mar. (1997), pp.2590-2595
[19]Flack, W.W., White, S., and Todd, B., “Process Characterization of One Hundred-Micron Thick Photoresist Films,” SPIE Microlithography, #3678-49 (1999)
[20]Frazier, A.B., “The Use of Polyimide for the Development of Micromachined Materials, Processes and Devices,” Ph.D. diss., Georgia Institute of Technology, 1993
[21]Wang, M.T., Tsai, M.S. and Liu, C., “Effect of Corrosion Environments On The Surface Finishing Of Copper Chemical Mechanical Polishing,” Thin Solid Films, Vol.308-309 (1997), pp.518-522
[22]Ozisik, M.N., “Heat conduction”, Second Edition, New York, John Wiley & Sons, 1993