A novel thermally evaporated etching mask for low-damage dry etching

DOI:
10.1109/TNANO.2017.2662218

Document Version
Accepted author manuscript

A novel thermally evaporated etching mask for low-damage dry etching

Hanbin Wang, Yiming Wang, Gengchang Zhu, Qingpu Wang, Qian Xin, Lin Han, and Aimin Song, *Senior Member, IEEE*

***Abstract*—Dry etching is widely used for nanofabrication and it requires reliable etching masks. However, hard dry etching masks usually need high-temperature and/or plasma deposition, which may causes damage to temperature-sensitive materials and semiconductor surface. Here, we develop a novel etching mask material, silicon monoxide (SiO), which is thermally evaporated and hence can avoid such drawbacks. The etching selectivity of evaporated SiO is shown to be higher than 50:1, comparable to sputtered SiO_2. A nanochannel device, called self-switching diode (SSD), is fabricated to evaluate the mask-deposition-process damage because of its high sensitivity to the process damage. In comparison to commonly used sputtered SiO_2 and polymethyl methacrylate (PMMA) mask, the SSD fabricated using evaporated SiO exhibit the highest channel conductance, strongest nonlinearity, and best high-frequency performance. Hall measurements also reveal that the carrier mobility of nanochannels etched with SiO mask is twice that of similar channels with SiO_2 mask.**

***Index Terms*—Silicon monoxide, Dry etching, Etching mask, Nanoscale device, Self-switching diode**

I. Introduction

With the rapid scaling of semiconductor devices, device channels have become nanometer scaled wires, fins or column [1, 2, 3]. Dry etching or reactive-ion etching is essential to define these nanochannels via top-down techniques. However, dry etching of nanoscale channels on sensitive materials, like III-V, oxide and organic semiconductors, are still challenging due to the restriction of etching mask. Photoresists and electron-beam resists are commonly used as dry etching mask because of their process feasibility. However, these organic resists have low etching resistance and are not suitable for nanoscale structures with high aspect ratio. The thickness of resists has to be reduced to guarantee the small line width in lithography, which makes organic masks not capable of protecting the semiconductors beneath them during dry etching process [4]. Although some electron-beam resists, such as spin on glass (SOG) could be used as hard mask and show superior dry etching resistance [5], the high cost and poor storage stability impede its pervasive application. Metal masks have already been widely used in the fabrication of micro-electro-mechanical systems (MEMS) or waveguides [6-8]. However, they are not suitable for all device etching, because the afterwards removal may etch or oxidize some semiconductors. Inorganic dielectric masks are more commonly used for nanochannels' dry etching. Many inorganic dielectric materials, such as SiO_2, SiN_x and Al_2O_3, have been extensively studied and widely used [9-11]. However, they usually need plasma and/or high-temperature deposition, like sputtering, plasma-enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD), which have non-negligible effect on sensitive materials. The plasma deposition has been found to cause severe damage to the surface of semiconductors and deteriorate the performance of devices, especially those with active layer close to surface [12-15]. High-temperature deposition may cause temperature-sensitive materials, for instance oxide semiconductors or organics, degenerate or deform. Furthermore, the flammable or toxic reaction gases in ALD make the deposition process very dangerous.

Here, we introduce a novel dry etching mask material- silicon monoxide (SiO) for the fabrication of nanochannels on sensitive semiconductors. SiO has been used as dielectric layer in MOSFET, protection layer on Graphene and anode materials in Li-iron battery. The SiO mask can be deposited by thermal evaporation while keep the substrate at room-temperature. This process not only avoids inducing damage to the surface of semiconductors, but also is feasible to organic substrates. In this work, detailed characteristics of SiO mask have been performed in comparison with the commonly used polymethyl methacrylate (PMMA) and SiO_2 masks. In order to evaluate the possible damage to host material during deposition process, a nanochannel device- self-switching diode (SSD) was fabricated because of its high sensitivity to any process damage [16-18]. SSD is a novel unipolar device and has amount of advantages including broadband, zero threshold, low noise, and ease of integration, etc. The direct current (DC) and high-frequency performances of the SSDs fabricated with different etching mask materials are compared in this study, and the possible physical mechanisms are analyzed with the assistance of Hall measurements.

This work has been supported by the Engineering and Physical Sciences Research Council (EPSRC) (Grant Nos. EP/G03737X/1 and EP/N021258/1), National Basic Research Program of China (Grant No. 2016YFA0301200), and National Natural Science Foundation of China (Grant Nos. 11374185 and 11304180).

Hanbin Wang, Yiming Wang, Gengchang Zhu, Qingpu Wang, Qian Xin, Lin Han, and Aimin Song are with the Center of Nanoelectronics and School of Microelectronics, Shandong University, Jinan 250100, China (e-mail: sduwhb@gmail.com; wym@sdu.edu.cn; zhugengchang@yeah.net; wangqingpu@sdu.edu.cn; xinq@sdu.edu.cn; hanlin@sdu.edu.cn; a.song@manchester.ac.uk).

Aimin Song is also with the School of Electrical and Electronics Engineering, University of Manchester, Manchester M13 9PL, U.K.

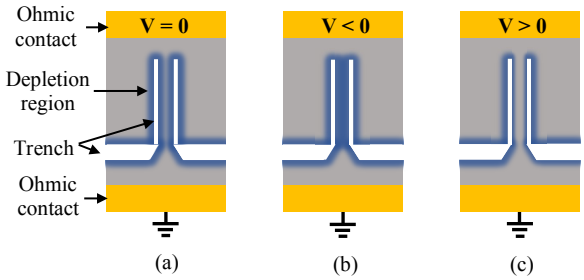

Fig. 1. Schematic illustration of SSD. (a) At zero bias, the nanochannel is partially depleted due to the surface states. (b) At bias $V < 0$, the nanochannel is fully depleted as the electrostatic field effect increases the width of depletion region inside the channel. (c) At bias $V > 0$, the nanochannel is opened because the electrostatic field reduces the depletion region.

II. Experimental Procedure

A. Preparation of SiO mask

High purity (99.95%) SiO powder was put in the tungsten boat which was connected to the electrodes in the vacuum chamber of HHV Auto 306 thermal evaporator. The chamber pressure was then evacuated to 2×10^{-6} Torr and kept below 1×10^{-5} Torr during the evaporation to prevent the SiO film from residual gas contaminating. The deposition rate was 1 Å/s and the final thickness was 50 nm. Patterns of SiO mask was transferred through exposed PMMA E-beam resist using an Oxford Pro 100 ICP-RIE system. And the etching recipe of SiO was the same as that of SiO_2. The etchant gases were CHF_3 and Ar with the flow ratio of 1:4. The etching pressure was 5 mTorr. The ICP power was 300 W to generate stable and repeatable plasma, and the RF power was 5 W to minimize the plasma damage to the underneath InGaAs layer.

B. Fabrication of InGaAs SSDs

SSDs were fabricated to investigate the effects of thermally evaporated SiO mask on the properties of nanoscale devices. The SSD is a unipolar two-terminal device. It consists of two insulating L-shaped trenches opposite to each other, creating a semiconductor nanochannel between them as shown in Fig.1. At zero bias, the nanochannel is close to pinch-off by the surface states as illustrated in Fig. 1(a). A negative bias ($V < 0$) further depletes the channel and results in a zero or low current, whereas a positive bias ($V > 0$) counteracts the lateral depletion and widens the effective width of the channel to enable a large current to flow. This results in a diode-like nonlinear current–voltage (I-V) characteristic.

The substrate of SSDs was epitaxial InGaAs grown on InP substrate and, from bottom to top, includes a 300 nm InAlAs buffer layer, a 15 nm InGaAs channel layer, a 15 nm InAlAs barrier layer and a 10 nm InGaAs cap layer. A sheet dopant of silicon with the density of 6×10^{18} cm^{-2} was introduced 5 nm deep in the cap layer. The carrier density and electron mobility of the channel layer, calculated by Hall measurements at room temperature, were 1.87×10^{12} cm^{-2} and 1.01×10^{4} cm^2/Vs respectively. Fabrication of devices started with insulating 20-μm-wide mesa by $H_3PO_4/H_2O_2/H_2O$-based wet etching.

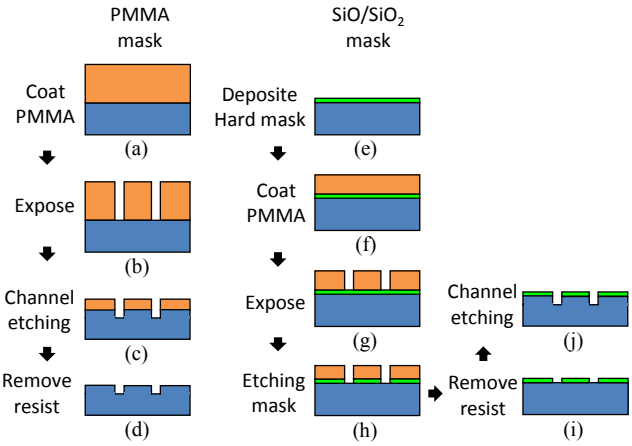

Fig. 2. Schematic illustration of SSDs channel fabrication processes with different masks. (a) – (d) are with PMMA mask. (e) – (j) are with SiO or SiO_2 mask. (a) Spin coat 450 nm PMMA. (b) Expose and develop PMMA. (c) Dry etch InGaAs channel, the thickness of PMMA also reduced during etching. (d) Remove PMMA residue with oxygen plasma. (e) Deposit SiO or SiO_2 film. (f) Spin coat 230 nm PMMA. (g) Expose and develop PMMA. (h) Dry etch SiO or SiO_2 film with PMMA as mask. (i) Remove PMMA with oxygen plasma. (j) Dry etch InGaAs channel.

Then, Au/Ge/Au/Ni/Ti/Au was evaporated successively followed by a 400 ºC RTA process at N_2 atmosphere to form ohmic contacts.

The following SSD channel etching was the most important process. Different etching procedures were used for three different masks: spin coated PMMA, thermally evaporated SiO and RF sputtered SiO_2. Fig. 2 depicts a schematic illustration of channel fabrication processes. For the devices with PMMA mask, a 450-nm-thick PMMA layer was spin coated. After being exposed by Raith E-line plus E-beam exposure machine and developed in a mixture of MIBK and IPA with the ratio of 1:3, the PMMA mask was hard baked at 110 ºC for 30 mins in oven to increase its etching resistance. Whereas, for the devices with SiO or SiO_2 etching mask, 50-nm-thick mask was deposited onto substrate, firstly. Then 230-nm-thick PMMA was spin coated. Patterns on SiO or SiO_2 were transferred from the exposed PMMA resist by dry etching using the SiO_2 etching recipe as mentioned before. The etching rate of SiO and SiO_2 was 13 nm/min and the selectivity of PMMA to silox was 2:1. Oxygen plasma ashing was executed to remove the PMMA resist and the generated polymer. Finally dry etching was performed to produce the trenches of all three devices. The etchant gases were CH_4, H_2 and Ar at the flow rates of 10, 30 and 10 sccm, respectively. The ICP power was 300 W to produce high-density plasma and the RF power was 5 W to minimize the etching damage. The etching rate of InGaAs was 14 nm/min, and the depth of etched trenches was about 100 nm. In all the dry etching processes as mentioned above, the absolute value of the bias voltages were kept below 110 V to minimize the bombardment of plasma to substrates.

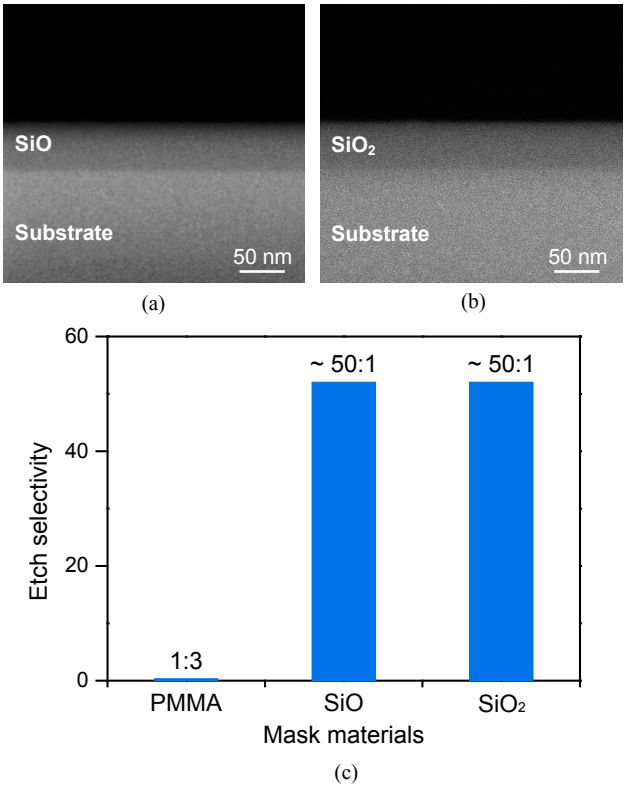

Fig. 3. (a) SEM image of the thermally evaporated SiO film. (b) SEM image of the RF sputtered SiO_2 film. (c) Etch selectivity of different mask materials to InGaAs.

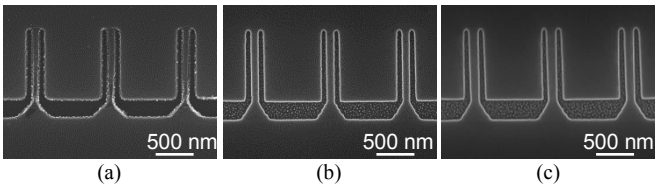

Fig. 4. SSDs dry etched with different masks. (a) SEM images of SSDs etched with 450 nm PMMA mask. SSD channels are bend because PMMA mask was softened during the etching. (b) SSDs etched with SiO_2 mask. (c) SSDs etched with SiO mask.

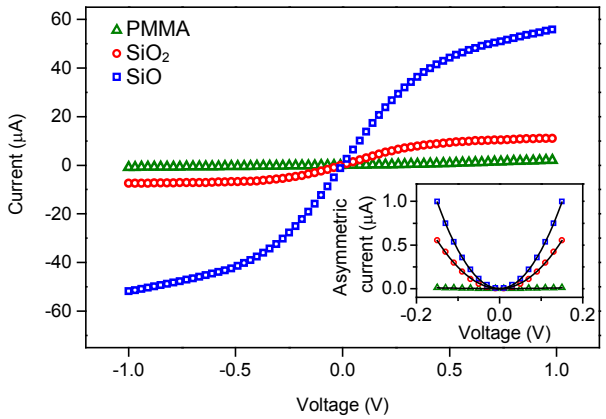

Fig. 5. Measured *I-V* characteristics of SSD with PMMA, SiO_2 and SiO mask. The inset figure is the extracted (symbols) and fitted (line) asymmetric component of the *I-V* curves.

TABLE I
EXTRACTED PARAMETERS FORM IV CURVES

Parameters at zero bias	PMMA mask	SiO_2 mask	SiO mask
R_0 (kΩ)	977	37.1	7.88
G_d (μS)	1.11	28.0	78.4
G'_d (μA²/V)	0.78	49.0	88.2

R_0, G_d and G'_d are resistance, differential conductance and curvature, at zero-bias, respectively.

III. Results And Discussion

A. Prosperities of thermally evaporated SiO

In Fig. 3(a), the Scanning Electron Microscope (SEM) image of 50-nm-thick thermally evaporated SiO shows comparable uniformity as that of RF sputtered SiO_2 thin films on silicon substrates, as shown in Fig. 3(b). The crystal size of SiO film, as reported by Klaus [19], is no larger than 2 nm. The small grain size of SiO film is very favorable to nanofabrication.

To compare the dry etching resistance of SiO mask to traditional masks, E-beam resist PMMA, SiO_2 and SiO were dry etched simultaneously with the same InGaAs SSD trench etching condition. The etching selectivity, defined as the ratio of InGaAs etch rate to that of masks, are showed in Fig. 3(c). The results show that PMMA has a low etching selectivity ratio of 1:3, whereas both evaporated SiO and sputtered SiO_2 have a much higher selectivity ratio of over 50.

B. Different masks on the properties of SSDs

The morphology of InGaAs SSDs dry etched with PMMA, SiO_2 and SiO masks were compared, as shown in Fig. 4. The designed width of SSD channels and trenches were 125 nm and 40 nm, respectively. The channel length was 1 μm. In Fig. 4(a), the SSD channels are crooked and the edges of channels are rough. These may due to the softening and erosion of PMMA mask during dry etching. As measured by SEM, the thickness of remained PMMA mask after etching is only 1/3 of the initial value. Besides the thickness, the geometric shape of PMMA mask was also changed during the dry etching as a result of ion bombardment and plasma heating effect, which is commonly observed in dry etching process with organic resists because of their poor etching resistance and low soften temperature [20]. As a contrast, the SSDs etched with SiO_2 and SiO hard masks show very good morphology. The channels are straight and the edges of trenches are smooth.

DC electrical characteristics of the SSDs with different etching masks were measured separately, as shown in Fig. 5. The inset figure in Fig. 5 shows the asymmetric current ($I_{asymmetric}$) of SSDs extracted from the *I-V* curves using the following equation: $I_{asymmetric} = [I(-V) + I(V)]/2$, where $I(-V)$ and $I(V)$ are the current of devices under backward and forward bias, respectively. The symbols in the figure are experimental results and the solid lines are fitted quadric curves. The good matching of measured results with fitting curves confirms that all SSDs work in triode-region mode [21]. The extracted zero voltage differential conductance $G_d = \frac{dI}{dV}\Big|_{V=0}$

and curvature $G_d' = \left.\frac{\mathrm{d}^2 I}{\mathrm{d}V^2}\right|_{V=0}$, where V is the applied DC bias and I is the current from I-V curves [22], are listed in Table I. Both G_d and G'_d of the SSD with PMMA as mask are much lower than the devices with hard masks. This is caused by the damage of channels during dry etching because of PMMA mask's poor etching resistance.

As a novel ultrahigh frequency diode, SSD is a very promising candidate for THz detector. The responsivity of RF detectors, which is defined as the ratio of output DC voltage over input signal power, is a key parameter to evaluate its detecting ability. Fig. 6(a) shows the zero bias responsivity of SSDs with signal frequency ranged from 10 GHz to 220 GHz at room temperature. Both the SSDs fabricated with PMMA and SiO_2 masks present obvious decrease in responsivity to the increasing frequency. Whereas the SSD with SiO mask shows constant responsivity through the full frequency range. This result indicates that the thermally evaporated SiO etching mask benefits the high frequency performance of SSDs.

Apart from responsivity, noise-equivalent-power (NEP) is another key factor in evaluating RF detectors. Fig. 6(b) shows the thermal NEP of SSDs with different masks calculated from the equation: $\mathrm{NEP} = \frac{\sqrt{4kTR_0}}{\eta}$, where k is the Boltzmann's constant, T is the absolute temperature, R_0 is the zero-bias resistance as listed in Table I, and η is the measured responsivity in Fig. 6(a). Compared to the SSDs with PMMA or SiO_2 mask, the SSD with SiO mask show much smaller NEP, especially at high frequency of 220 GHz. The maximum NEP of the SSD with SiO mask was about 400 pW/Hz$^{1/2}$, which is 1-2 orders of magnitude smaller than those of the other two. This was contributed by the higher responsivity of the SSD with SiO mask at high frequency and smaller resistance at zero bias. The NEP of the SiO masked 3-channel parallelized SSD was a little higher than that of commercial Schottky diode, which usually is less than 50 pW/Hz$^{1/2}$. However, this will not limit the application of SSD detectors, because the final NEP value is reasonably low due to their easy integration in parallel [23, 24].

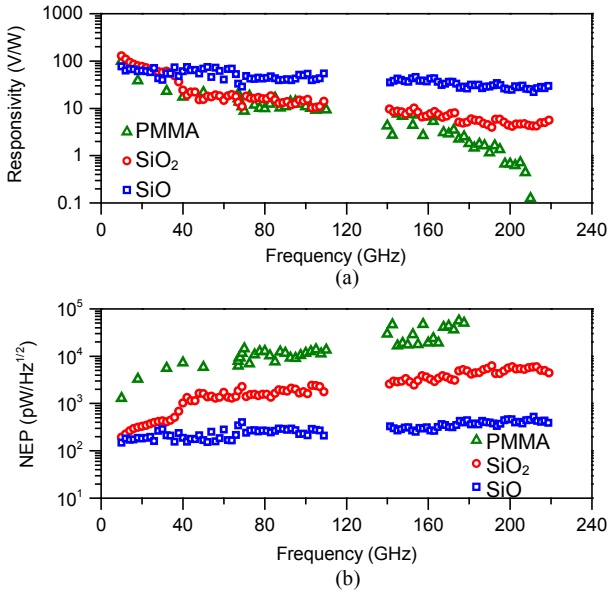

Fig. 6. Responsivity and NEP of SSDs fabricated with different masks. (a) Measured zero bias responsivity at room temperature. (b) Calculated thermal NEP with responsivity results.

C. *Hall bar fabricated with SiO and SiO_2 masks*

To explain the reasons for better high frequency performance of the SSD with SiO mask compared to that with traditional SiO_2 mask, nanoscale Hall bars were fabricated with SiO_2 and SiO masks using the same substrate and process conditions for SSDs. Fig. 7 shows SEM image of the fabricated Hall bar. The width of hall bars were ranged from 100 nm to 200 nm and the etching depth was 100 nm.

Measured carrier density (n) and hall mobility (μ) at room temperature are listed in Table II. Both the carrier density and mobility of hall bars fabricated with SiO_2 mask are smaller than those with SiO mask. The mobility of the former is only half of the latter. This is due to the plasma damage caused during the sputtering-deposition process of SiO_2. Katsushiko *et al.* pointed out that the ion bombardment from SiO_2 deposition could induce damage to substrates [25]. Tsubaki *et al.* reported that the damaged depth in semiconductors after depositing SiO_2 with RF sputtering could be as large as 150 nm [12]. The deposition-induced damage of sputtered SiO_2 mask decreases the carrier density and mobility of devices, and, as a result, the high frequency performance of the devices with SiO_2 mask is

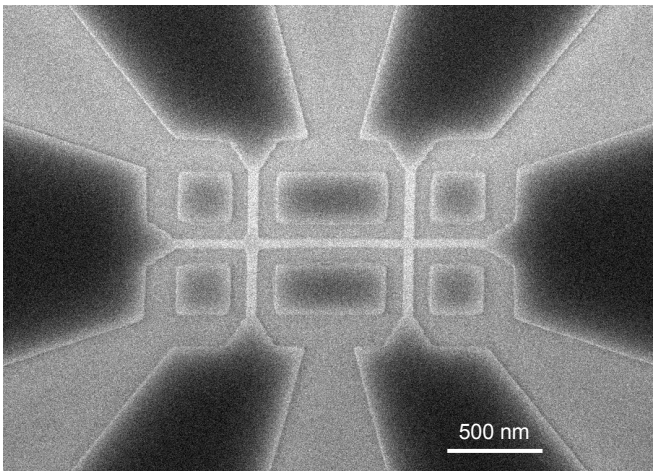

Fig. 7. SEM image of fabricated nanoscale Hall bar with SiO mask.

TABLE II
MEASURED CARRIER DENSITY AND HALL MOBILITY OF HALL BARS WITH SiO_2 AND SIO MASK AT ROOM TEMPERATURE.

Channel width (nm)	SiO_2 mask		SiO mask	
	n ($\times 10^{12}$ cm^{-2})	μ cm^2/Vs	n ($\times 10^{12}$ cm^{-2})	μ cm^2/Vs
100	1.72	465.37	2.23	1031.04
125	1.62	473.55	2.28	1056.05
150	1.62	515.95	2.06	1152.61
200	1.66	484.06	2.40	1025.65

The magnetic field was 0.52 T.

influenced. Whereas, as the benefit of the damage-free thermal evaporated SiO, the devices with SiO mask present much better performances.

IV. Conclusion

A novel thermally evaporated dry etching mask material, SiO, is developed. Its detailed characteristics have been performed and compared with the commonly used PMMA and SiO_2 masks. The PMMA mask showed much less etching resistance than hard masks and, as a result, both the DC and high-frequency performance of the SSD fabricated with PMMA mask are very poor. Although the evaporated SiO and sputtered SiO_2 masks showed similar etching resistance and produced nanoscale features with good morphology, the nanochannel conductance of the SSD with SiO mask is substantially higher than that with SiO_2 mask. Hall measurements reveal that the carrier mobility of nanochannels etched with SiO mask is twice of the channels with SiO_2 mask. Furthermore, at high-frequency characterizations of SSDs up to 220 GHz, the responsivity of the SSD with SiO mask was 6 times better than that with SiO_2 mask. In conclusion, SiO is promising dry etching mask material because of its easy-deposition, high-performance and low-damage thermal evaporation process to the host materials.

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