NACK NETWORK

Building College-University
Partnerships for Nanotechnology
Workforce Development

Dielectrics by Growth and Deposition

Outline

- Introduction – Silicon Dioxide
- Types of Oxide
- Furnace Deposition
  - Dry Oxidation
  - Wet Oxidation
- High Pressure Oxidation
- Chemical Vapor Deposition
- Modifying Dielectric Constant

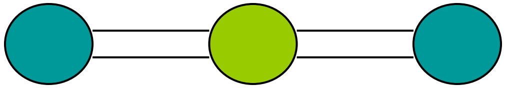
Oxidation

- Oxidation is a chemical reaction in which silicon and oxygen form a stable material called silicon dioxide

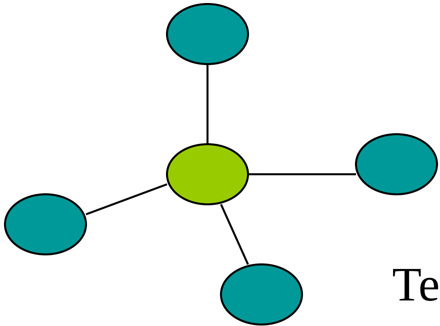
Silicon Dioxide

- A high quality, stable electrical insulator material
- Grows naturally on silicon
- Has many uses

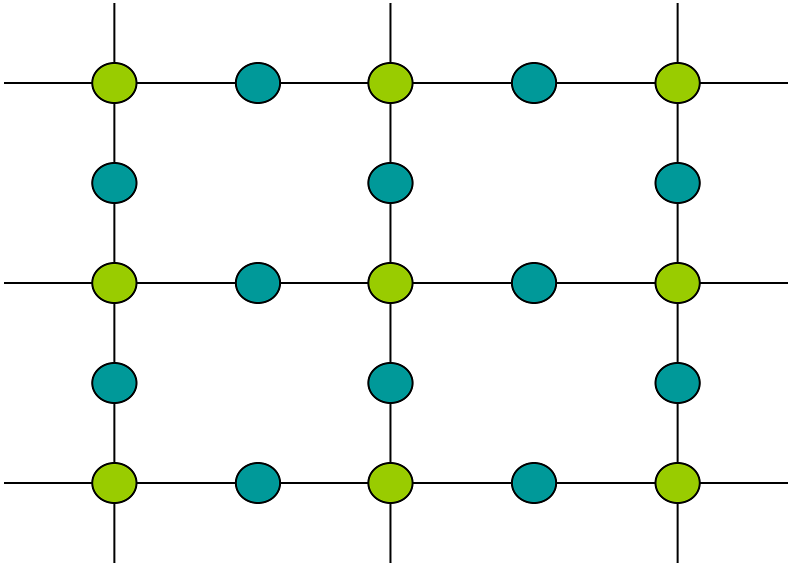
Silicon Dioxide



SiO_2



Tetrahedral
Structure of oxide



Oxide Lattice

Key:
Oxygen ●
Si ●

Oxide Quality

- Determined by checking:
  - Film thickness and uniformity (nm)
  - Defects (#/volume)
  - Dielectric strength (MV/cm^2)
  - Stress (MPa)
  - Interface properties

Film Thickness

- Oxide film thickness can be roughly judged by the color of the oxide
- This is a general measurement, but can be useful

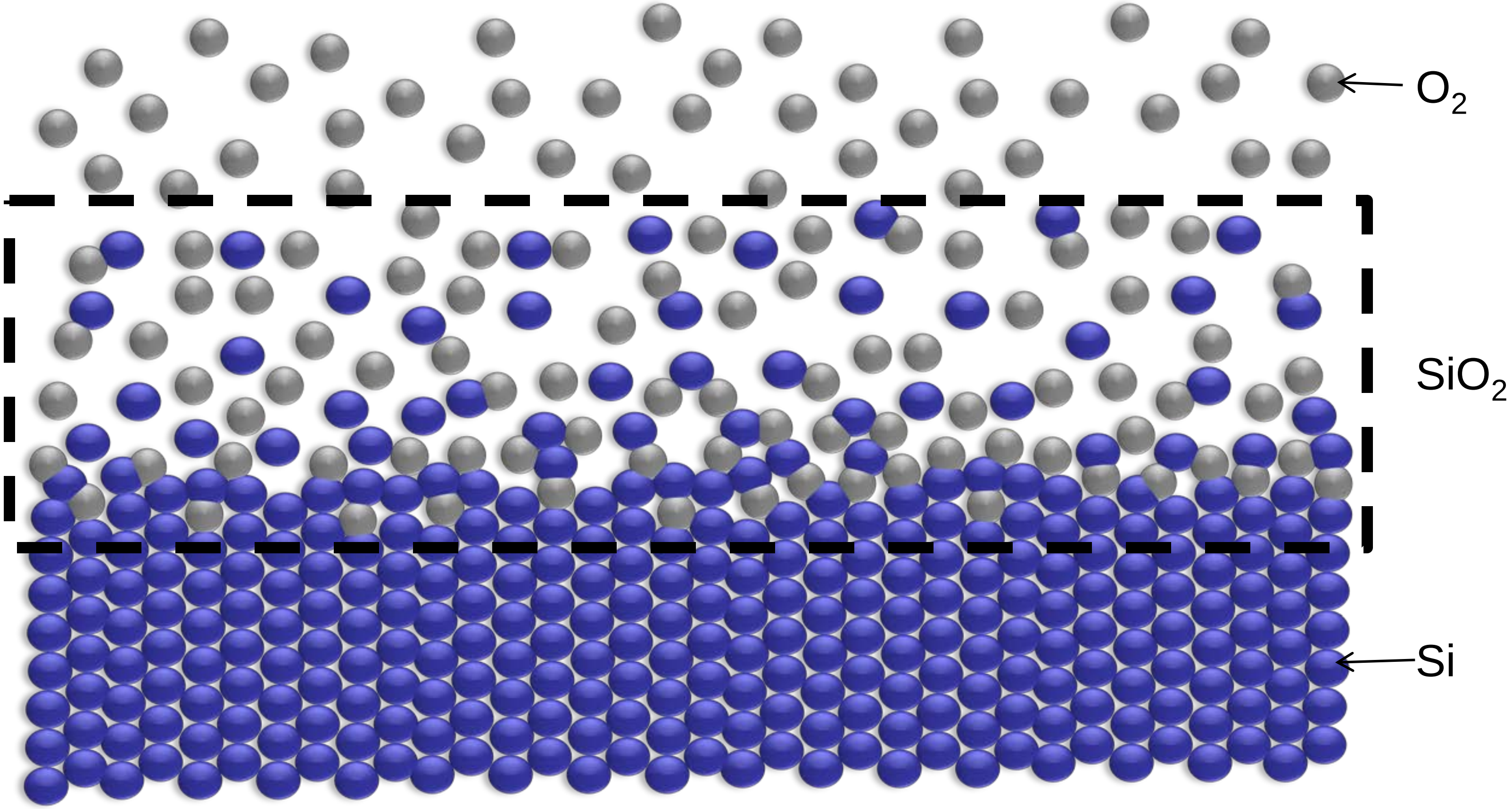
Silicon Dioxide Thickness

Thickness	Color	Thickness	Color
0.05 µm	Tan	0.54	Yellow-green
0.12	Royal Blue	0.57	Yellow to “yellowish”
0.17	Metallic to v. light yellow-green	0.60	Carnation Pink
0.22	Gold w/ orange-yellow	0.63	Violet-red
0.27	Red-violet	0.80	Orange
0.32	Blue to Blue-green	0.85	Dull, light Red-violet
0.36	Yellow-green	0.87	Blue-violet
0.39	Yellow	0.92	Blue-green
0.42	Carnation Pink	0.97	Yellow to “yellowish”
0.50	Blue-green	1.00	Carnation Pink

Mechanism

- Oxygen moves through the oxide layer to react with the silicon below
- Oxygen diffuses from an area of high concentration (gas) to an area of low oxygen conc. (silicon)
- Fick's first law states that the particle flow per unit area, J (particle flux), is directly proportional to the concentration gradient of the particle:
  - $J = -D\partial N(x,t)/\partial x$

Diffusion of Oxygen



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Mechanism

- Silicon in the wafer is consumed as the oxide grows
- Typically, for every 1000Å of oxide grown, 400Å of silicon is consumed
- For a 1000Å layer of oxide, the wafer physically grows only 600Å

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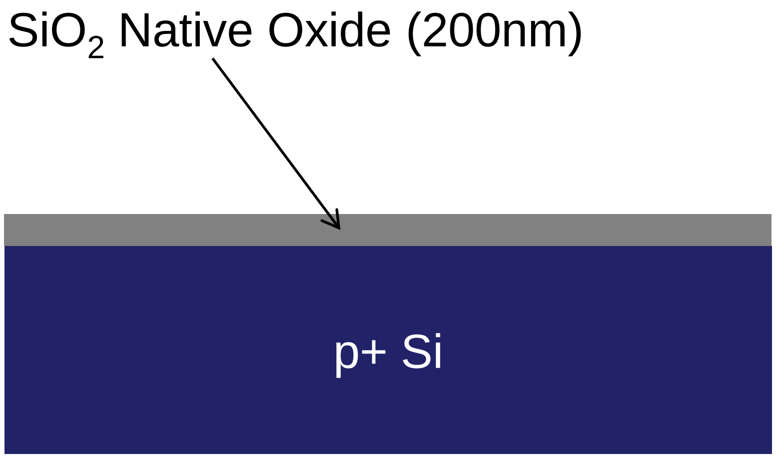
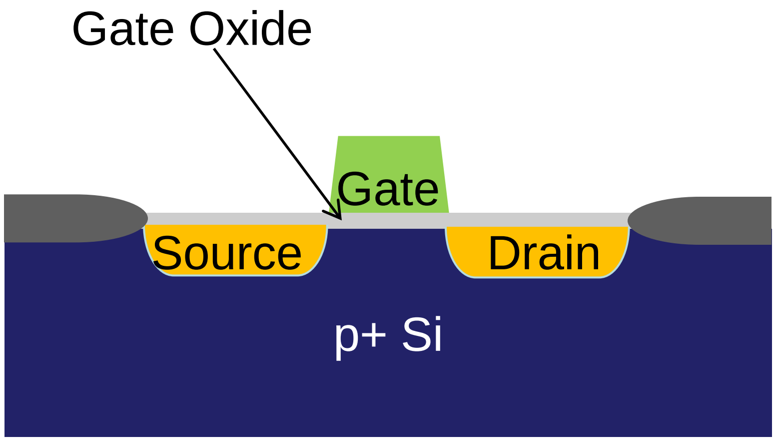
Types of Oxides

- Native Oxide
  - Considered a contaminant. It grows naturally on silicon at room temperature due to the presence of O_2 in the ambient environment
  - Can reach a maximum thickness of ~40Å
- Gate Oxide
  - A highly pure, specifically grown oxide that acts as a dielectric between the gate, source, and drain on the MOS structure
  - Optimal thickness is between 20Å and several hundred Å
  - Higher purity and thinner oxides lead to the production of faster devices

Types of Oxide





Native Oxide

Gate Oxide

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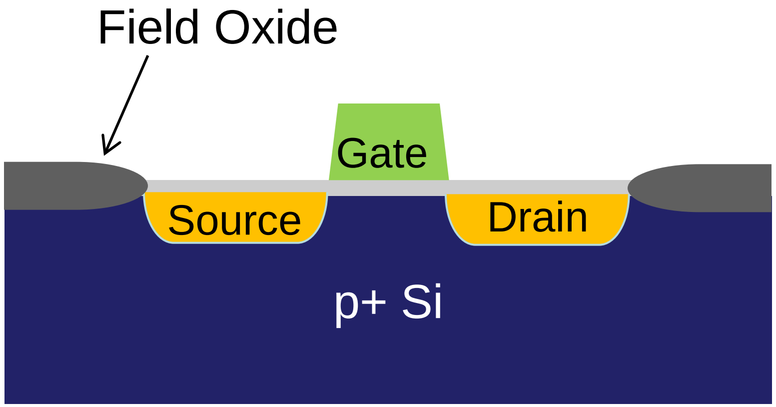
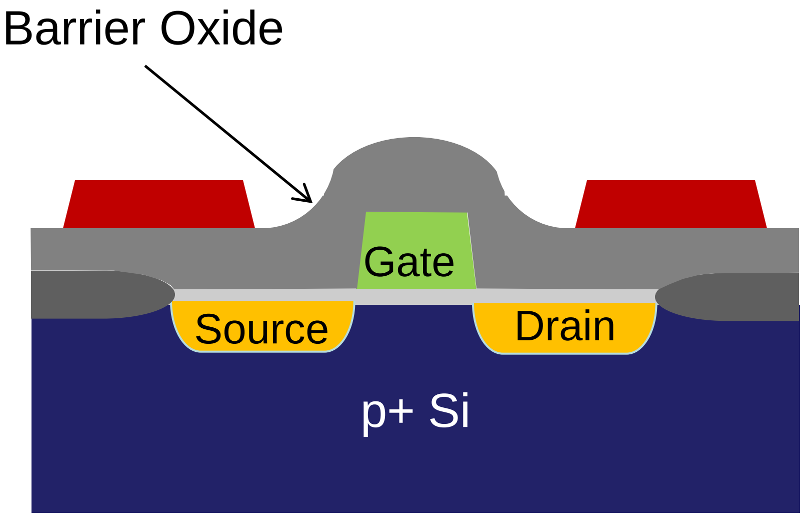
Types of Oxide

- Field Oxide (FOX)
  - Used to isolate individual transistors from each other on a wafer
  - Ideal thickness is between 2,500Å – 15,000Å.
- Barrier Oxide
  - Protects active devices and silicon from further processing
  - Ideal thickness is usually several hundred Å

Types of Oxide



Field Oxide

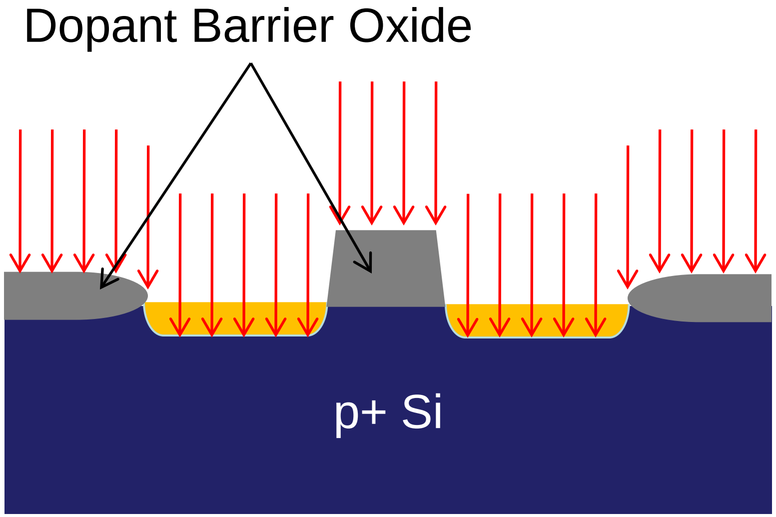


Barrier Oxide

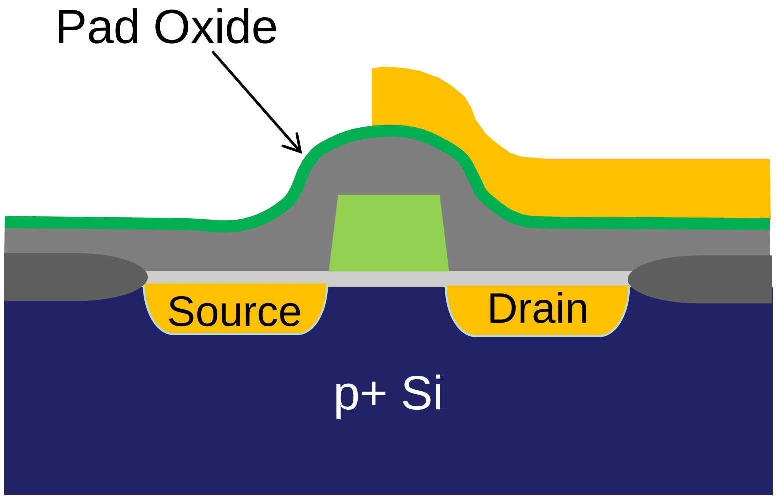
Types of Oxide

- Dopant Barrier
  - Used as a mask to prevent doping in unwanted areas
  - Also used in patterning of wafers. Its chemical resistance provides a strong barrier for etching/depositing/etc. patterns in a wafer
  - Optimal thickness ~400Å – 1,200Å, but it depends on the doping process
- Pad Oxide
  - Reduces stress for Si_3N_4
  - Thickness is kept very thin

Types of Oxide



Dopant Barrier Oxide

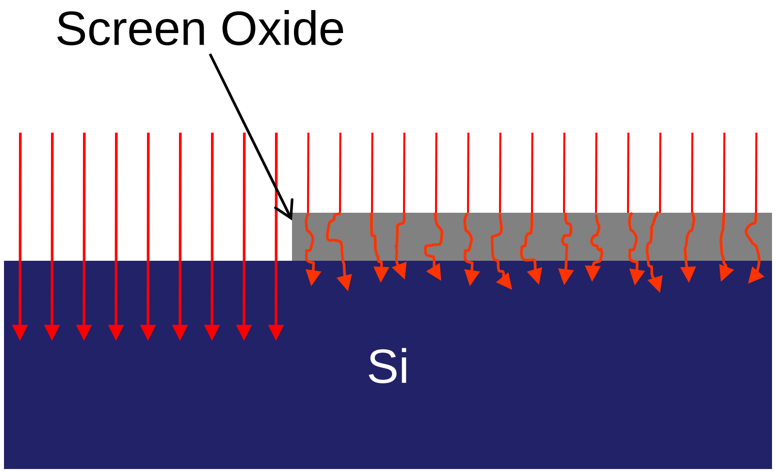


Pad Oxide

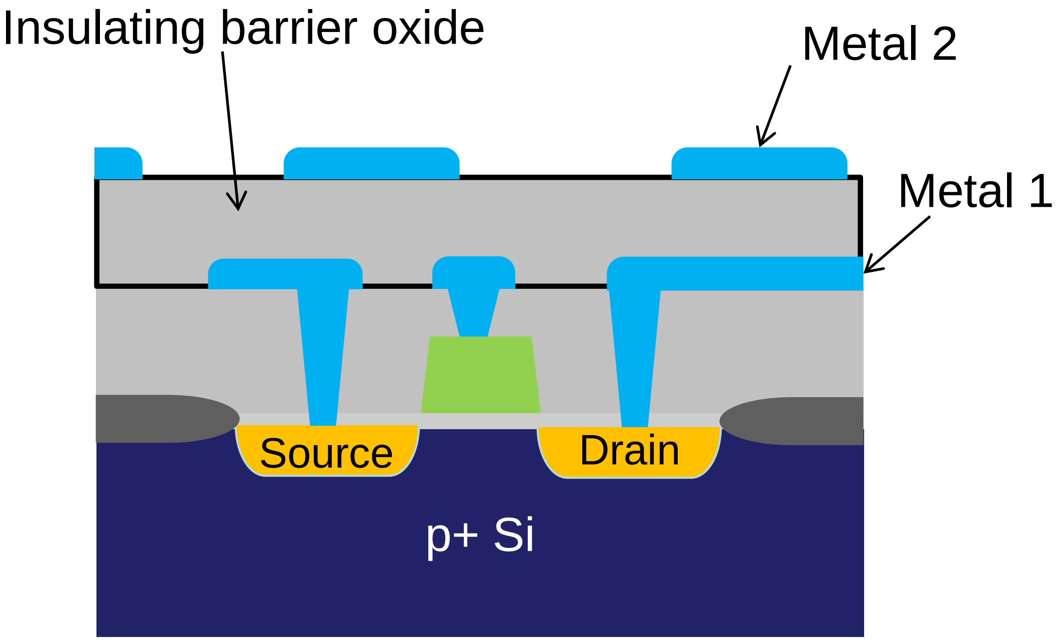
Types of Oxide

- Implant Screen Oxide
  - Used to prevent/minimize implant channeling and damage
  - Thickness varies depending on implant depth
- Insulating Barrier
  - Placed between metal layers to prevent electrical shorts
  - Used because of its insulating properties (does not conduct electricity)
  - This layer is deposited (as opposed to grown) and the required thickness varies

Types of Oxide



Implant Screen Oxide



Insulating Barrier Oxide

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Oxidation

- Three methods for **growing** oxide:
  - High temperature oxidation (furnace)
    - w/ oxygen: dry oxidation
    - w/ steam: wet oxidation
  - High-pressure oxidation – HiPOx
- One method of **depositing** oxide:
  - CVD – chemical vapor deposition

Furnace Oxidation

- Important parameters for furnace processes:
  - Time
  - Temperature
  - Temperature gradients
  - Gas composition and purity
  - Gas flow rate
  - Thermal stress management

Dry Oxidation

- Oxidation that occurs as a result of oxygen reacting with silicon
  - $Si + O_2 \rightarrow SiO_2$
- Grows high quality thin layers of oxide (i.e. gate oxides)
- Grows oxide at a slow rate

Dry Oxidation

- The process is performed in the furnace at a high temperature (normally above 1000^{o}C)
- Uses oxygen as the process gas
- May use HCl in process to reduce charges at the wafer surface

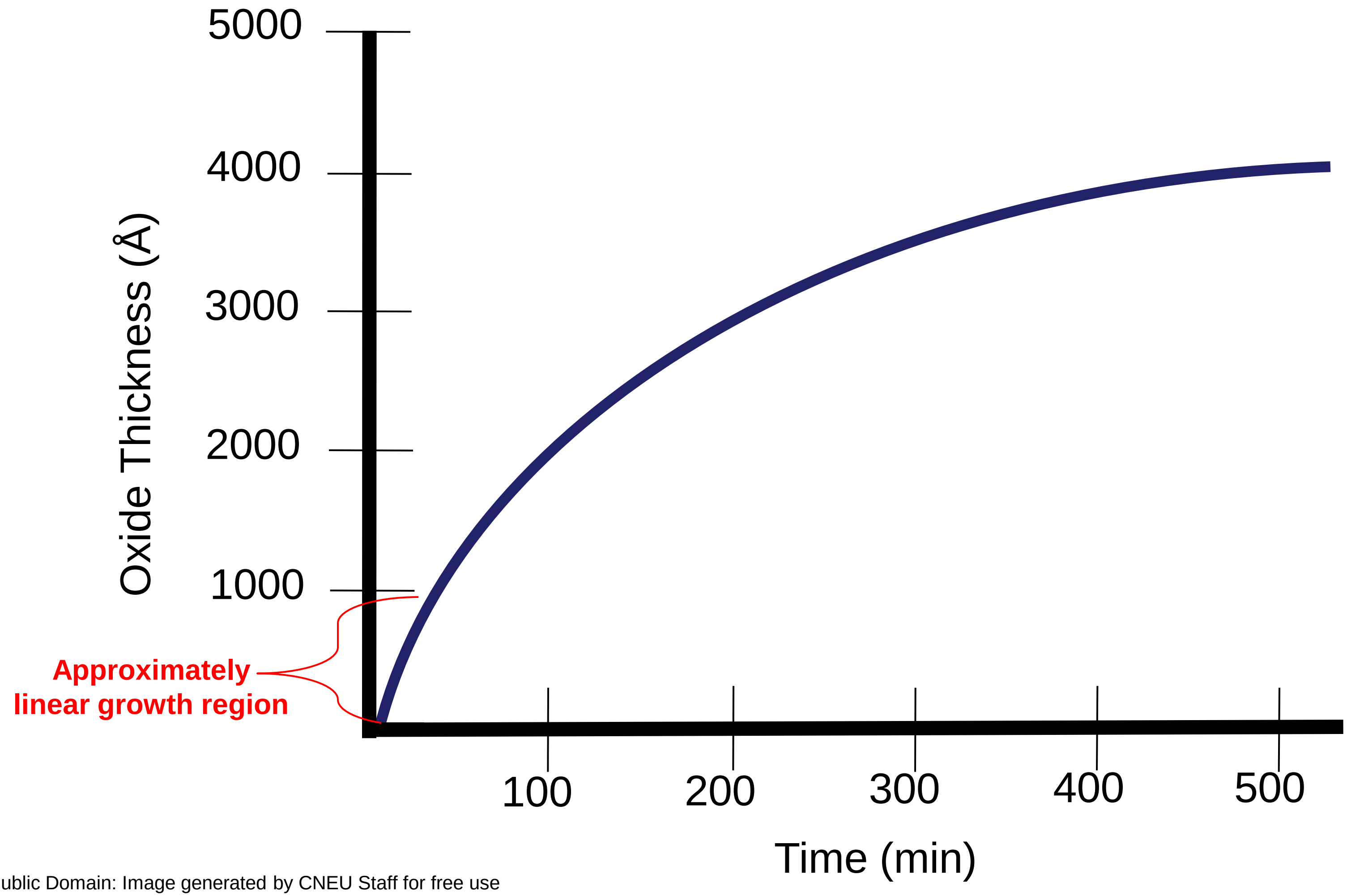
Dry Ox. Process Recipe

Step	Time (min)	Temp. (°C)	Gas Flow (SLM)		
			N_2	O_2	HCL
1) Idle state		850	3	0	0
2) Push wafer into furnace	5	850	3	0	0
3) Ramp up temp.	15	10°C/min	3	0	0
4) Temp. stabilization	5	1000	3	0	0
5) Dry oxide growth	30	1000	0	2.5	.067
6) Anneal	30	1000	3	0	0
7) Ramp down temp.	75	-2°C/min	3	0	0
8) Retrieve wafer	850	3	0	0	

Ramping

- With any furnace process, temperatures need to be changed slowly when wafers are present
- The ramp-up rate (in this recipe) is 10^{o}C/min. The ramp-down rate is –2^{o}C/min.
- These slow rates are necessary to prevent warping or other thermal stress problems in the silicon wafers

Dry Ox. Growth Rate



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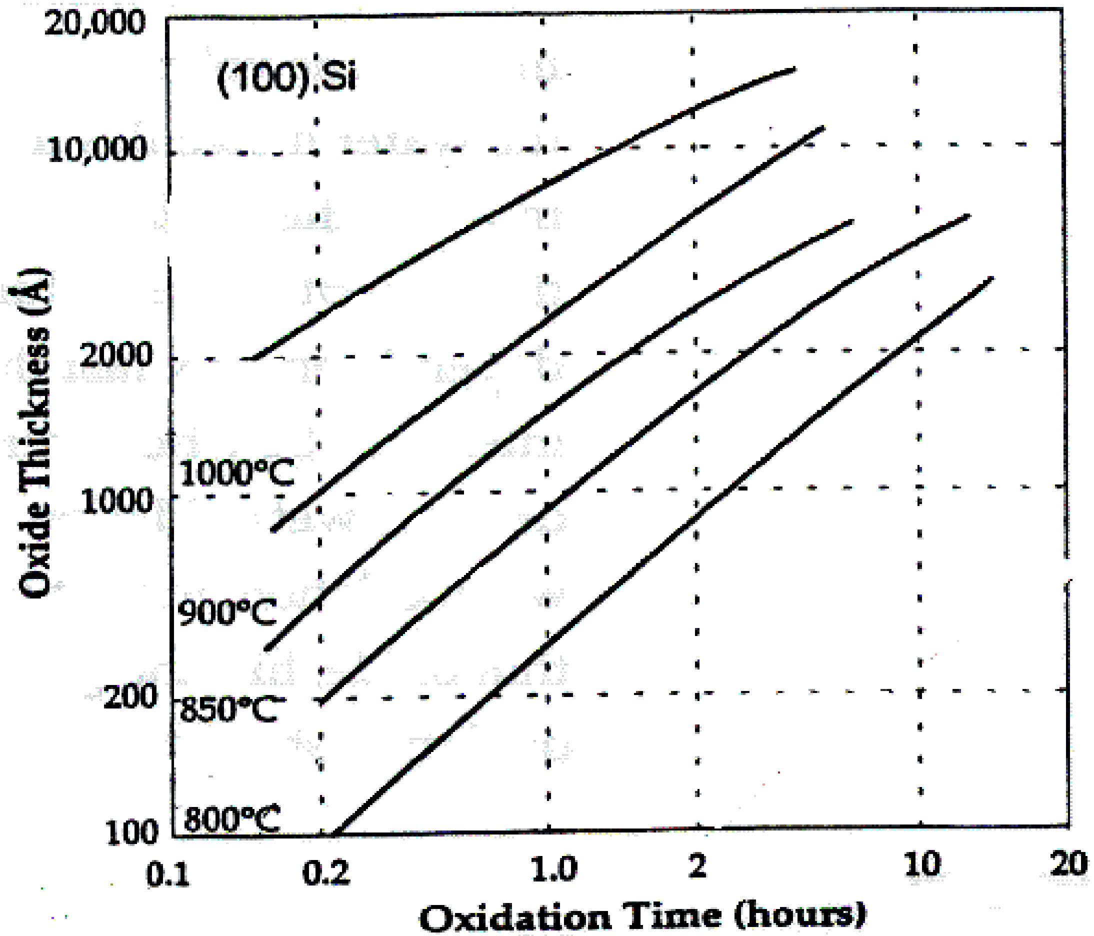
Wet Oxidation

- Oxidation that occurs as a result of steam reacting with silicon
  - $Si + 2H_2O \rightarrow SiO_2 + 2H_2$
- Uses steam as the process gas
  - Steam is pyrolytic meaning that in high heat H_2 and O_2 are reacted together to create water vapor molecules
  - This produces a much purer steam for oxidation
- Grows oxide at a much faster rate and produces a lower quality oxide
- Use this technique when very thick oxides (i.e. field oxide) are needed rather than high quality

Chlorinated Agents

- Using chlorinated gases in the oxidation process can neutralize charge accumulation at the silicon oxide interface
- Chlorinated agents are kept under 3% so instability is not created in the oxide layer
- Chlorinate agents can increase growth rates by 10-15%. This mechanism is poorly understood
- Trichloroethane (TCA), an organochloride, offers low corrosion to the oxidation system

Wet Ox. Growth Rate



Wet Vs. Dry Oxidation

- Dry Ox. Grows higher quality oxides
  - In Wet Ox., steam reacts with silicon and produces hydrogen molecules. These molecules become trapped in the oxide and change the stoichiometry of the oxide
    - Stoichiometry indicates how closely the deposited film approaches the ratio of the elements given by its chemical formula

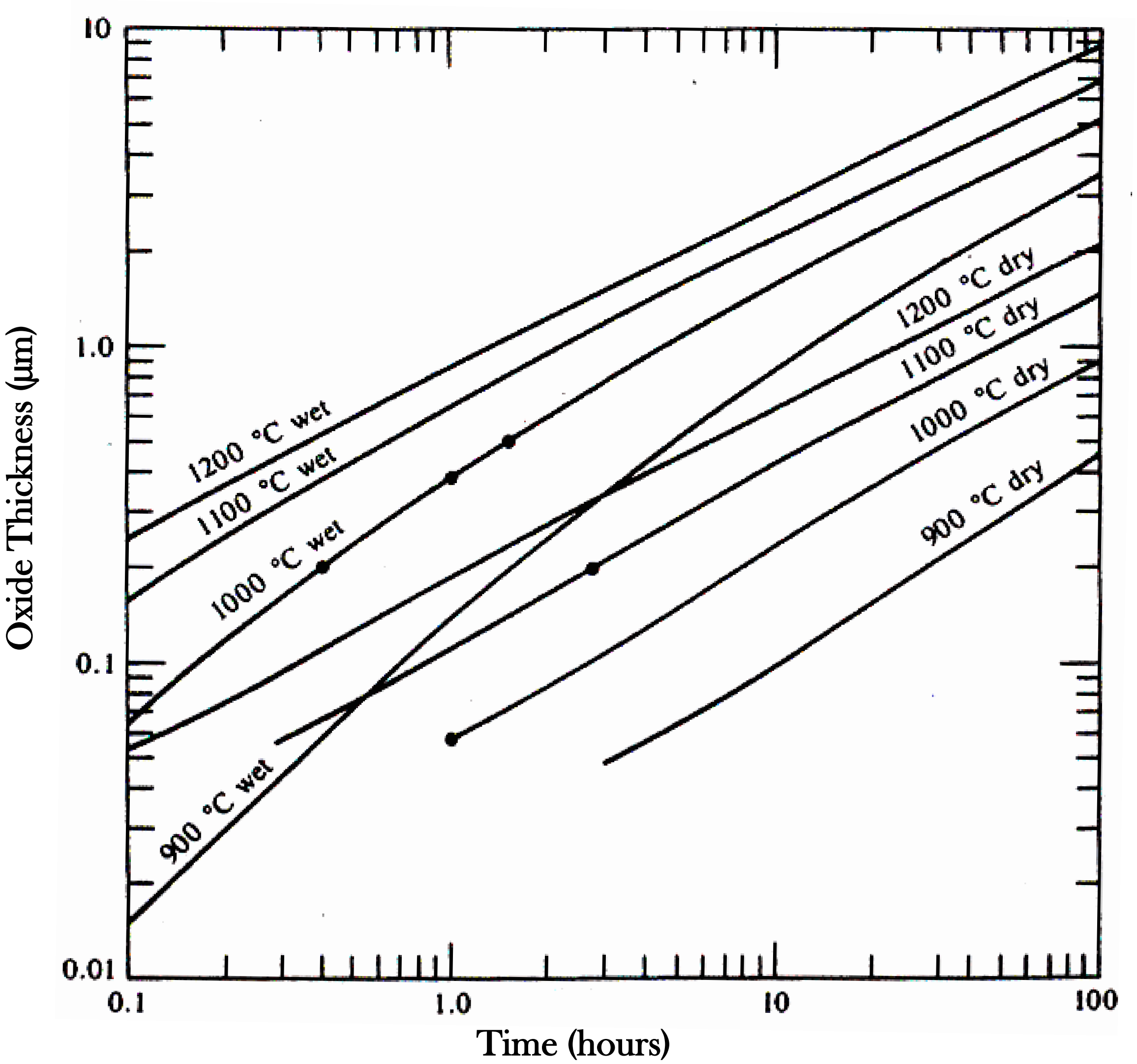
Wet Vs. Dry Oxidation

- Wet Ox. grows oxides faster
  - At 1000^{o}C, the solubility of water in silicon (total amount of water that can be present in a certain volume of silicon) is 600 times that of oxygen in silicon
  - Even though oxygen diffuses faster, it has a lower solubility and physically can fit fewer atoms in the silicon

Wet Vs. Dry Oxidation

Oxide Type	**Temp (°C)**	**Thickness (Å)**	**Time**
Dry	1000	1000	2 hours
Wet	1000	1000	12 minutes

Wet and Dry Oxide Growth



Increasing Temp. – Decreasing Time

- There are many problems with increasing the temperature at which a process runs
  - Increased diffusion of impurities present in the wafer
  - Crystal defects (stacking faults)
  - Permanent damage from thermal stress
  - Equipment damage/more costly equipment to run at higher temperatures

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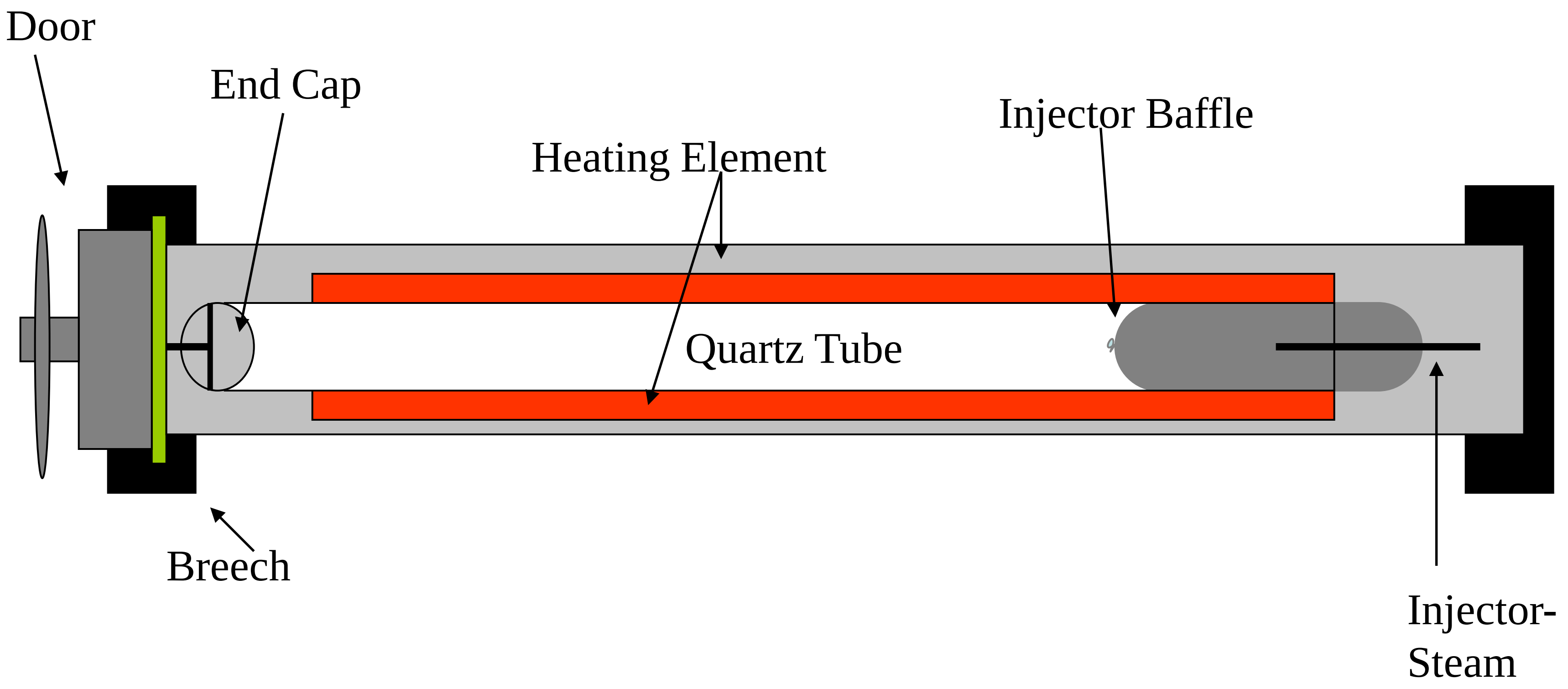
High Pressure Oxidation - HiPOx

- Used to grow thick layers of oxide in reduced time and temperature (i.e. field oxide)
- Uses steam and oxygen as process gases
- Has special HiPOx system equipment

HiPOx System



HiPOx

- Runs at reduced temperatures:
  - ~ 650^{o}C – 900^{o}C
- And increased pressures:
  - ~ 5 – 20 atm

HiPOx Relationships

- Time and pressure are inversely related:

Temp. (°C)	**Pressure (atm.)**	**Time**
900	1	5 hours
900	5	1 hour
900	25	12 minutes

*Assuming that the wafers are of the same thickness

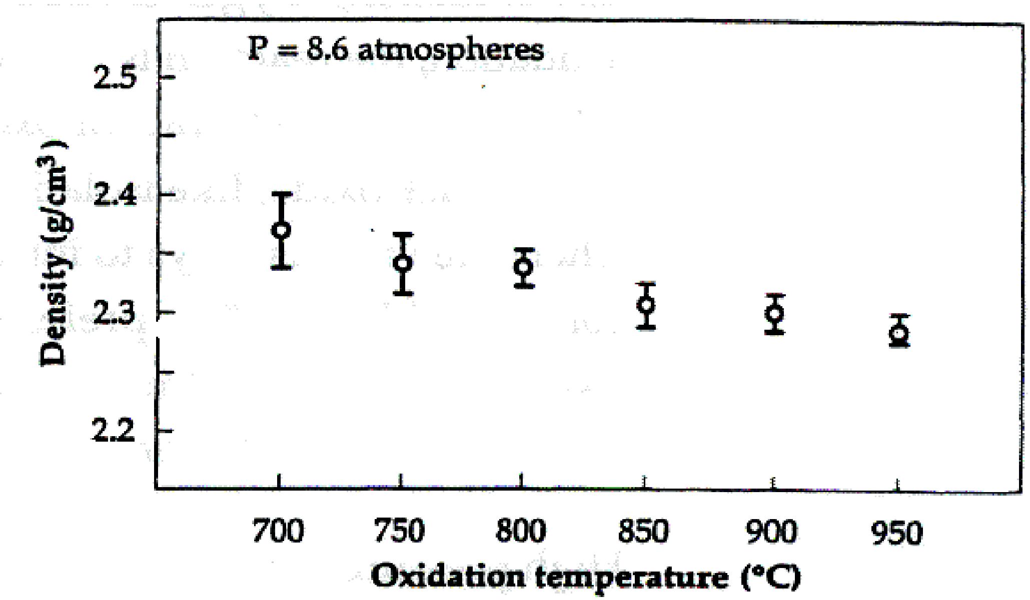
HiPOx Relationships

- Temperature and Pressure:
  - For every increase of one atmosphere, the temperature can be dropped by 30ºC to obtain the same thickness in the same time

Time (hours)	**Pressure (atm.)**	**Temp. (°C)**
5	1	1000
5	10	700

HiPOx Relationships

- Temperature and oxide density:
  - – As temperature decreases, oxide density increases



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CVD

- The deposition of oxide onto a wafer using the decomposition of silane
  - $SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$
- “Deposits” a layer of oxide as opposed to the other techniques that “grow” the oxide

CVD

- Oxide is deposited at ~ 350^{o}C
- Silicon and oxygen react in plasma and deposit onto the wafer (other techniques diffuse O_2 into the wafer and use the wafer's silicon to produce oxide)
- Creates a nearly stoichiometric layer

CVD

- Nitrous oxide (N_2O) or carbon dioxide (CO_2) are actually preferred over oxygen
- The oxygen reacts too easily in the plasma and can cause poor film quality

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Engineering Dielectric Constant (k)

- This concept centers around capacitance (C) and its relationship to signal time (T) when fabricating integrated circuits

$$C = \frac{k\varepsilon_o A}{d}$$

- k= dielectric constant
- ε_o= permittivity of free space (constant)
- A= area
- d= distance between features

Engineering Dielectric Constant (k)

- Signal Time (T)

$$T = RC$$

- R= resistance of metals
- C= capacitance
- In IC fabrication, the idea is to use the correct dielectric material with the right constants for a desired process
  - Keeps the capacitance the same to insure the signal time is not compromised

Engineering Dielectric Constant (k)

- Interconnects- wiring
  - The wire lines must be as close as possible in order to fit the maximum amount of transistors on a chip
  - The distance must be minimized, therefore; the dielectric material must have a low k
  - As d decreases, k must also decrease

Low k Dielectric Materials

- FSG, k = 3.4-4.1
- HSQ, k = 2.9
- Nanoporous silica, k = 1.3-2.5
- Fluorinated polyimide, k = 2.6-2.9
- PTFE, k = 1.9
- DVS-BCB, k = 2.65
- Aromatic hydrocarbon, k = 2.65

Engineering Dielectric Constant (k)

- Gates
  - Uniformity is a key quality parameter
  - It is easier to make the gates thicker, to insure that any variation in uniformity won’t impact device performance as drastically
  - Example 1: If a gate is 30Å:
    - Material uniformity that varies by 10Å drastically alters performance
  - Example 2: If a gate is 100Å
    - Material uniformity that varies by 10Å does not impact performance that drastically

Engineering Dielectric Constant (k)

- Gates
  - – A thicker gate requires a dielectric material with a high k value
  - – As d increases, k must also increase

High k Dielectric Materials

- Ta_2O_5, k = 22-30
- TiO_2, k = 20-85
- Nb_2O_5, k = 11
- HfO_2, k = 17
- Y_2O_3, k = 15