Machine Aligned Fabrication of Submicron Nb/Al-AlO_X/Nb Junctions using a Focused Ion Beam

R.B. Bass, A.W. Lichtenberger

Department of Electrical Engineering, University of Virginia, Charlottesville, VA 22903

1. Introduction

In this abstract, a process is described that we are developing which uses a Ga^+ focused ion beam (FIB) for the fabrication of Nb/Al-AlO_x/Nb superconductive-insulating-superconductive (SIS) tunnel junctions. The objective is to use a machine alignment scheme for the definition and insulation of junctions with diameters as small as 0.5μm for high critical current density (J_C) applications. The fabrication of such ultra-small area SIS junctions has typically only been achieved using electron beam lithography and a multi-resist layer scheme [1]. Typical techniques for the fabrication of SIS junctions use a self-aligned resist lift-off process. The resist pattern is used to define both the junction counter electrode and the subsequent insulation field that insulates the base electrode from the wiring layer. The wiring layer contacts the junction counter electrode through a via in the insulation field that is created during resist lift-off.

Figure 1 shows a Nb based self aligned trilevel resist junction insulation process, which is used in this laboratory for fabricating micron-scale SIS junctions. As can be seen from the figure, the trilevel resist is used both as the etch mask for the junction counter electrode (Fig. 1a) and as the deposition mask to the SiO insulation layer (Fig.1b) so that a via in the SiO is created after lift-off (Fig.1c) to the top of the junction Nb counter electrode. A subsequent Nb wiring layer can then interconnect different junctions and electrical elements on the wafer [2]. Generally, such self-aligned insulation processes are effective for junctions sizes on the order of a micron or larger [3]. As junction sizes are decreased; however, the lift-off process becomes more difficult to perform and from our experience, it becomes inherently more difficult to successfully insulate the junction for the wiring step. With conventional lithography,

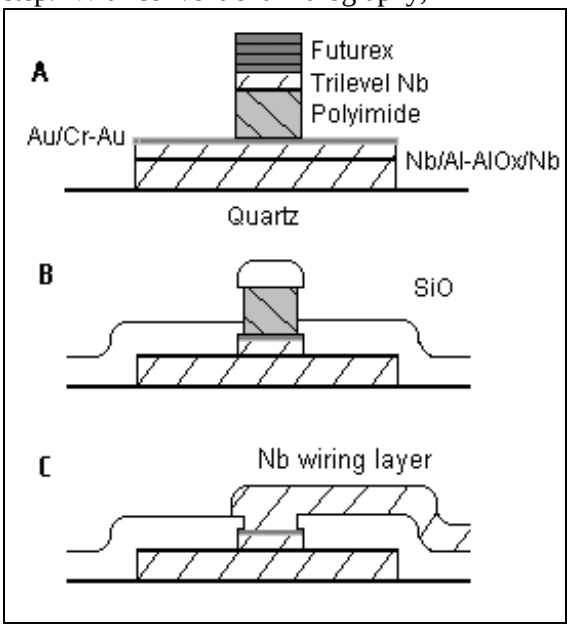

Figure 1 (A) Self-aligned trilevel (Futurex/Nb/Polyimide) sitting atop an unetched SIS junction. (B) SiO shown covering an etched SIS junction. (C)The SiO is then lifted-off from atop the junction, allowing the Nb wiring layer to contact the junction.

it also becomes more difficult to accurately define junctions smaller than 1 μm with a resist feature that is also compatible with the lift-off of the thick junction-insulation layer. Conceptually, an alternative to such a self aligned process is a machine aligned method where the Nb junction

etch and the SiO insulation and via definition steps are decoupled. Such a process, which decouples the two steps, is very attractive for several reasons: (1) it allows the use of different lithography processes for the two steps, (2) the junction should be very well insulated since it is initially totally "buried" by the insulation layer and (3) it avoids the use of any lift-off processes.

The main drawback with such a process is while for large area junctions the alignment, definition and etching of the required insulation via to the Nb junction counter electrode is feasible, for small junction areas the alignment tolerances are critical. For a 0.5µm diameter junction with a 0.2µm diameter via hole, the via must be aligned to better than 0.15µm in order for the via hole to be registered only on top of the junction. Such tolerances are beyond most commonly used lithography tools.

2. Machine Aligned FIB Technique

We are investigating a machine aligned junction insulation process where the critical alignment and via definition is accomplished with a Ga^+ FIB etching system. The FIB used in this research is an FIB 200 Series Workstation manufactured by FEI Company [4]. Incorporating the FIB into the fabrication process allows for the alignment of sub-micron features, which is not feasible with optical lithography alone.

In this process, the Nb junction counter electrode is defined and insulated in a separate step. This permits the use of, in our case, a thin DUV resist with good resolution of half-micron feature sizes that would otherwise not be suitable for a full self-aligned junction insulation process. After stripping the resist, the junctions are "buried" with a blanket evaporation of 1000-3000Å of SiO over the entire wafer (Fig. 2a). A thin layer of Cr (350Å) is then deposited on top of the SiO to improve the imaging capabilities of the Ga+ beam in the FIB system. The excellent registration and anisotropic etching capabilities of the FIB system are then used to etch a hole in the Cr film directly above the junctions. Alignment is feasible due to the outline of the junction perimeter that is transferred through the SiO layer for registration. The FIB is controlled such that the etch is through the thin Cr mask layer but not totally through the much thicker SiO insulation layer. (Fig. 2b). The Cr then serves as a mask for an anisotropic CHF_3 reactive ion etch (RIE) of the SiO via. In our process a thin $Cr_{0.1}$-$Au_{0.9}$ layer was previously defined on top of the junction counter electrode to serve as an etch stop for the CHF_3 RIE as well as to promote adhesion between the counter electrode and the Nb wiring layer [5]. The Cr mask layer can now be removed with a simple wet etch before the deposition and definition of the Nb wiring layer, which contacts the Nb junction counter electrodes through the SiO vias (Fig. 2c). To date, via features as small as 200nm have been easily formed using the FIB. The ion column of the FIB uses an ultra-rigid mechanical assembly to ensure beam position and high resolution images, allowing for spot diameters down to 30nm [4]. We therefor anticipate the capability to define via holes smaller than 100nm.

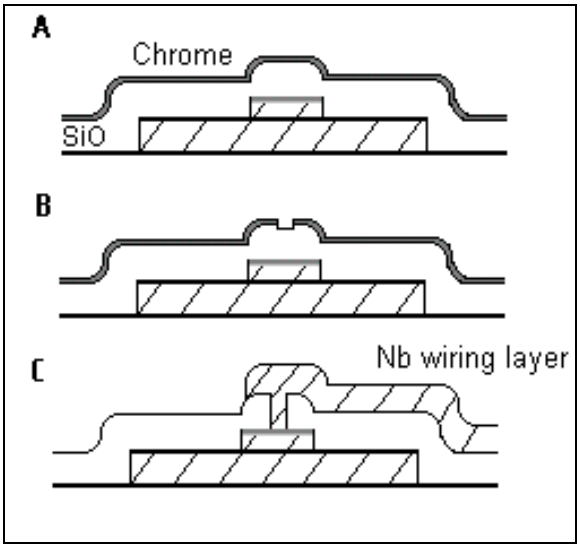

Figure 2 (A) SiO is allowed to deposit directly on top of the SIS junction along with a thin Cr layer. (B) The Cr is then patterned using the FIB. (C) A subsequent RIE of the SiO allows the Nb wiring layer to be contacted to the junction.

To facilitate the control of the FIB Cr etch, an end point detection (EPD) program is used during the etch. The EPD indirectly detects the type of material being milled by measuring the amount of current ejected from the wafer surface during the etch. For example, if the EPD program measures a drop in observed current during an etch, a transition from a conductive material to a less conductive material may be inferred. This tool is therefore very useful in controlling the duration of the FIB etch so that it does not proceed into the Nb counter electrode.

One drawback to this proposed machine aligned FIB junction insulation process is that while with common lithography techniques an entire wafer can be patterned with a single exposure, with the FIB process the SiO vias will be individually defined. It is not clear how robust the process is at this time and whether the etching of the via patterns in the Cr layer can be written and controlled by a computer program much like E-beam lithography.

It is also interesting to not that this technique of defining small insulation vias has an analogous application in the fabrication of Schottky barrier diodes. For the case of whisker contact diodes, the critical step in defining diode areas involves opening a small diameter via in an insulation field to a GaAs surface [6]. Schottky barrier contacts are then formed in a platting process defined by the insulation vias. The FIB SIS junction insulation process should be readily transferable to the fabrication of 100nm diameter whisker-contacted Schottky diodes. Since this application does not require any alignment, it is likely that an array of such via patterns can be "written" using the FIB in a reasonable time frame under computer control.

3. Summary

A new method for defining submicron SIS junctions has been described. Using the small Ga^+ beam size, anisotropic etching and precise alignment capabilities of the FIB system, a machined aligned insulation technique has been described. This new process will allow for the fabrication of sub half-micron junctions with high critical current densities. The use of the FIB system decouples the junction electrode and junction insulation steps and to avoid lift-off processes, which are problematic for submicron junctions.

4. References

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