Beam Lead Quartz Chips for Superconducting Millimeter-Wave Circuits

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ABSTRACT

The assembly of superconducting millimeter and submillimeter-wave circuits often requires RF ground connections. These are usually made by soldering, wire bonding, conductive adhesive or conductive wire gaskets. The difficulty of assembly increases with frequency as chip dimensions and tolerances shrink. The assembly issues, and also the throughput requirements of large radio astronomy projects such as ALMA (Atacama Large Millimeter Array), suggest the need of a beam lead technology for these circuits. Beam lead processes are already established for silicon and gallium arsenide wafers. However, niobium circuits on quartz substrates present unique difficulties. SIS junctions introduce additional thermal and chemical constraints to process development. For quartz, wet etches are isotropic and dry etches with high etch rates require large ion energies. Therefore, it is difficult to develop a conventional process in which gold pads on the substrate surface are formed into beam leads by a backside etch. Instead we have developed a topside process in which, after the mixer circuits are completed, dicing cuts are made at the finished chip dimensions but only partly through the wafer. The dicing cuts are then filled with a sacrificial material in a non-CMP process, and planarized. Gold plated pads are then defined, overhanging the planarized cuts. The sacrificial material is then removed from these cuts, leaving the gold beam leads. The wafer is then backside lapped into the cuts to the desired thickness, separating the individual chips. We discuss the new planarization scheme developed for this beam lead process and compare a variety of sacrificial materials.

Index terms - beam leads, Nb, SIS, quartz, epoxy

1. INTRODUCTION

In recent years millimeter and submillimeter-wave devices have been widely used in radio astronomy, remote sensing, material research, spectroscopic studies, various military applications and other fields. As the demand increases for better, more reliable millimeter and submillimeter-wave devices, a tremendous amount of design and development effort is being devoted to improving the performance and yield of these devices. Numerous ground-breaking performances have been reported recently. For instance, the high frequency limit of state-of-the-art MMIC amplifiers has been pushed to nearly 180GHz.[1] All-planar multiplied sources have been developed and demonstrated at frequencies up to 1.5THz.[2] Also, millimeter and submillimeter-wave Superconductor-Insulator-Superconductor (SIS) mixers, with sensitivity near quantum limit, have been demonstrated and used in many radio telescopes around the world.

Though these devices are capable of offering excellent performances at millimeter and submillimeter-wave regions, they are very difficult to fabricate and handle. This is because these circuits are extremely small and usually fabricated on very thin and fragile substrate materials such as silicon, GaAs or quartz. Also, as the frequency of circuits increases, the size of the circuit housing decreases, the tolerance required for the circuit housing increases and the placement of the circuit become very difficult and critical, making assembly of these devices even more problematic. All of these problems make replicating state-of-the-art millimeter and submillimeter-wave devices extremely difficult. To overcome these difficulties, the circuit mount has to be designed so that it is as simple as possible to fabricate and non-critical to the function of the circuit. Also, the assembly procedures must be as easy and reliable as possible.

There are several ways to mount millimeter and submillimeter-wave circuits into a package housing. Conductive adhesive has been used in some power device packages to provide better heat sinking to the circuits. A drawback to the conductive adhesive technique is that after the adhesive is set, it is difficult to remove the circuit from the package without damaging it. Also, applying the appropriate amount of adhesive at the intended places is not a simple task. Circuit mounting can also be accomplished solely by the attachment of the leads from the package to the electric traces of the circuit. With this design, the lead attachment provides the necessary mechanical, thermal, and electric connections to the circuit. There are several ways of attaching leads from a package housing to a circuit. Wire bonding and soldering are commonly used in the microwave and millimeter-wave industry. But, as the frequency of circuits is increased, the electrical trace of the circuit is reduced. Some of the circuit traces of millimeter and submillimeter-wave circuits are so small ($< 25\mu m$) that it is very difficult to make a reliable wire bond (or solder bond) to the circuit. Also, as the frequency increases, the required bond wire length becomes shorter and more critical. This makes attaching the leads to the circuit very difficult. In general, wire bonding and soldering can be used in assembling millimeter and submillimeter-wave circuits, but they are not without their own share of difficulties.

Conductive adhesive, wire bonding, and soldering all attach leads permanently to the circuit. None are ideal for prototyping tasks where frequently changing circuits are needed. Several other mounting techniques offer easy circuit replacement. Micro-spring contact, formed by pressing an extremely narrow (0.125mm in diameter) gold- plated beryllium copper wire against the gold-plated circuit trace pad, has been successfully used in packaging Josephson and SIS mixer chips.[3,4] However, micro-spring contacts are usually not as robust as those formed by wire bonding and soldering. Also, the initial fine adjustment of the micro-spring wire may be very time- consuming. But since it is very easy to replace a circuit chip in a micro-spring contact package, this method is particularly useful in prototyping low-power dissipation devices. Another good mounting technique uses conductive wire gasket contacts. This technique offers easy chip replacement capability and provides excellent mechanical, electric and thermal contact to the circuit. For our SIS mixer circuits, a quartz chip is clamped between the left and right block halves in a suspended-substrate stripline configuration. The RF and DC ground connections between substrate and block are achieved through two gold crush wires placed on the shoulders of the channel to contact metal pads on the substrate. The gold contact wires are compressed when the two halves of the block are assembled. Since the connections are made solely by compressing gold wires, the depth from the top surface of the lower half-block to the shoulder of the substrate channel becomes very critical. This technique has been applied successfully in packaging 200 to 300GHz SIS mixers for many years at NRAO.[5,6] However, due to the difficulties in machining substrate channels with required precision at higher frequencies, it may not be practical to use this technique in some submillimeter-wave circuits.

The most preferable method for packaging millimeter and submillimeter-wave circuits is the “beam lead” technique. This beam lead technique was developed in the 1960's as a simple and reliable way for connecting integrated circuits to printed circuit boards. In this approach, thick ($\sim 10\mu m$) metal lead contacts are formed directly on the circuit during the circuit fabrication process and become an integral part of the circuit. The metal lead patterns are formed to extend beyond the perimeter of the circuit. The beam lead circuits are usually packaged in a split block housing. Using the beam lead as a handle, the circuit can easily be picked up and placed into the substrate channel with the extended beam beads positioned in recesses around the channel so that it is self-aligned and suspended in the middle of the substrate channel. When the two halves of the block are assembled, the beam leads are clamped between two block-halves and held in place, thus providing both a good thermal and electrical connection to the device and a rigid physical support of the package.

Beam lead processes are well established for Si and GaAs wafers.[7-9] The beam lead technology for GaAs membranes has also been successfully developed recently for packaging a 1.5THz planar multiplied source.[2] Most of these processes use selective wet etches that take advantage of anisotropic etching of the substrate due to crystal plane orientation. In this case, Au beam lead patterns can be formed during or after completion of the wafer circuitry fabrication process. Since beam lead thickness on the order of $10\mu m$ is needed for consideration of physical robustness, these features are typically plated and can be formed directly on the surface of the wafer. The beam lead feature is then “revealed” to overhang the substrate with a backside wet etch. At present, no similar beam lead process exists for quartz wafers. The main obstacle is that thick quartz layers a) cannot be etched anisotropically by selective wet etch, and b) cannot be etched by conventional RIE, thus a backside etching cannot be adapted to fabricate beam leads for quartz wafers. However, because of its excellent millimeter and submillimeter-wave properties such as low dielectric constant,

low loss tangent and good thermal conductivity, quartz is the most preferable substrate material for superconducting millimeter and submillimeter waveguide circuits. It is, therefore, extremely desirable to develop a beam lead process for quartz wafers.

2. RESEARCH

Nb SIS circuits on quartz substrates present unique difficulties for beam lead processing. SIS junctions introduce additional thermal and chemical constraints to process development. Integral to the SIS device is a thin, typically oxidized, aluminum tunnel barrier on the order of 1nm thick. We have found that temperatures as high as 200C for 5 to 10 minutes have no adverse effects on the quality of the electrical characteristics of the junctions, other than introducing a slight increase in the normal resistance of the device. However, temperatures much higher, or for longer durations, will substantially degrade the electrical quality and significantly affect the normal resistance of the junctions. We have also found the electrical quality of our finished junctions is very sensitive to quartz (hydrofluoric acid-based) and gold (iodine-based) wet etches. As is discussed in subsequent sections, this requirement places significant limitations on our choice of materials and development of beam lead processing.

For quartz substrates, wet etches are isotropic and therefore unsuitable for use in a backside etch processes. With typical wafer thickness between 50 and 250μm, and beam lead overhangs on the order of 40μm, the geometry requires an anisotropic back side substrate etch. The use of a dry, RIE backside etch was considered. Conventional RIE etch rates of SiO_2 (quartz) are much too low to consider etching 50μm or more. High SiO_2 etch rates also require large ion energies resulting in a process that would be difficult to stop effectively on the "underside" of the gold (Au) beam leads. It may be possible to develop a process using an Inductively Coupled Plasma Reactive Ion Etching (ICP RIE) tool where much higher plasma densities result in dramatically higher etch rates at lower platter voltages. Oxford Plasma Technology offers a tool with an anisotropic quartz etch process for thicknesses on the order of 50μm. In such a process the beam lead metallization would be patterned on the quartz surface and a thick metal mask of Cr or Ni would be patterned on the back side of the wafer. The wafer would be mounted upside down on a carrier wafer followed by a backside ICP RIE etch through the entire quartz wafer and either into the carrier wafer or stopping on the 'underside' of the Au beam lead. In this process the ICP RIE etch would not only remove the quartz to reveal the beam leads but would also replace the customary dicing process. It is not clear if such an ICP RIE etch process would have a sufficiently high selectivity to Au, with respect to quartz, and an acceptable uniformity of quartz etching such that the Au beam leads would not be significantly and non-uniformly etched in the process. It is possible to envision a process where a more durable refractory metal is defined between the Au beam lead and the quartz substrate, but not under the Au contact to the wafer circuitry. Such a metal would provide suitable endpoint selectivity for the ICP RIE etch but would have to be removed from the underside of the Au beam lead following the ICP RIE process. Unfortunately our laboratory does not have such an ICP RIE tool with which to explore such a process.

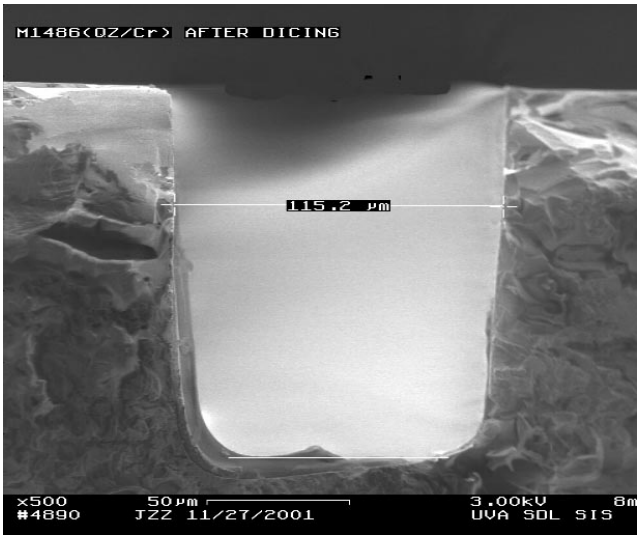

Figure 1. An SEM micrograph of the cross-section of a 125μm deep trench. The trench was diced in 250μm thick quartz with two dicing cuts.

2.1 Topside Process

Instead we have investigated a scheme that does not involve backside etching. Conceptually, the process envisioned is as follows: (1) after the mixer circuits are completed, dicing cuts are made at the finished chip dimensions but only partly through the wafer, (2) the dicing cuts are then filled with a sacrificial material, (3) the material is somehow planarized, and etched back to the quartz surface, (4) Au pads, in contact to the mixer circuitry, are defined that overlap the planarized cuts, (5) the wafer is then backside lapped into the cuts to the desired thickness, and (6) the

sacrificial material removed leaving the Au beam leads overhanging the dicing cuts, separating the individual beam lead chips. Steps 5 and 6 can be switched depending on material properties. This process uses the dicing saw to effectively perform the function of a backside etch before the beam leads are formed. The effective anisotropy of quartz removal by dicing is quite good, as is seen in Fig. 1. This scanning electron microscope (SEM) image shows a cross-section of a nominal 115µm wide channel formed with two adjacent dicing cuts. The slight taper in the channel is a result of the profile of the dicing blade. This effect is minimized by choosing a blade with a smaller kerf width and a minimum blade exposure. Using a smaller kerf width, however, requires multiple passes by the blade to define the channel.

The critical component of this scheme is the capability to fill the trenches and planarize back to the quartz surface. The process and materials need to be compatible with all the other material, thermal, and chemical demands of the remaining processes. Many materials and processes that might have been considered in order to accomplish the planarization requirement are not acceptable due to the constraints of subsequent processing steps.

2.2 Planarization Products

Much of our research has focused on developing a suitable planarization scheme. Two spin-on polymer products, NR9-8000 and PC3-6000 from Futurrex, Inc. were initially evaluated.[10] Polymer material is very attractive for this beam lead process as it is easily removed with liquid strippers. NR9-8000 is a negative tone photoresist used for thick film applications. It is sensitive to 365nm UV light. We intended to take advantage of the high resolution, low viscosity and excellent re-flow characteristics at 150C of this resist.

Spin-application of the resist at 300rpm results in a 50µm thick film, which is then baked, exposed and developed leaving patterns of resist inside the dicing channels. Because of small amounts of inorganic content in NR9-8000 and the resultant resistance to oxygen etching, it is important that the mask linewidth is chosen such that the resist remains entirely inside the channel and not covering the surface of the wafer. Planarization is obtained with a 150C postbake of the resist. The post bake causes the resist to re-flow, filling the channel. Resist thickness, as well as channel width and depth must be closely controlled so that the appropriate volume of resist is available to fill the trench volume. In Figs. 2 and 3, typical profiles are shown from the same wafer, where in one case too much resist and in the other too little resist was defined within the channel. It is suspected that this variation is partly due to differences in the actual width of the dicing channel from cut to cut. It is interesting to note that the resist tends to stay in the channel due to surface tension, even when the channel is overloaded with resist. This amount of variation in planarization is unacceptable for our beam lead process.

PC3-6000 is an n-butyl acetate spin-on planarization coating designed for feature topographies on the order of only 10µm. PC3-6000 is spun on the wafer at 1500 rpm to a thickness of approximately 10µm and baked at 200C on a hotplate. Immediately upon baking, a large number of small air bubbles form in the coating and, over the next two minutes, coalesce to become larger. These bubbles are then 'dragged' off the wafer surface with pointed tweezers. After five minutes, the PC3-6000 surface becomes smooth and uniform and the wafer is slowly cooled to prevent the PC3-6000 from cracking. A surface profile of the resulting topography is shown in Fig. 4. The PC3-6000 is then etched

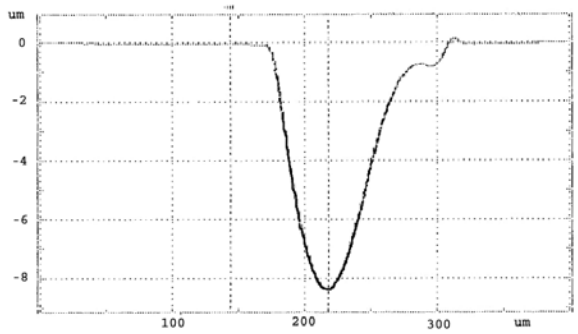

Figure 2. Surface profile over a dicing trench with too little NR9-8000 resist. The resist was baked for 3 minutes at 150C.

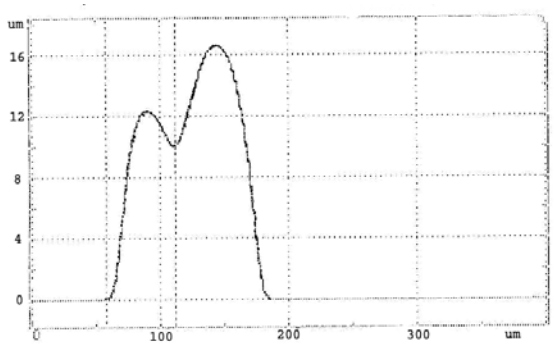

Figure 3. Surface profile over a dicing trench with to much NR9-8000 resist. The resist was baked for 3 minutes at 150C.

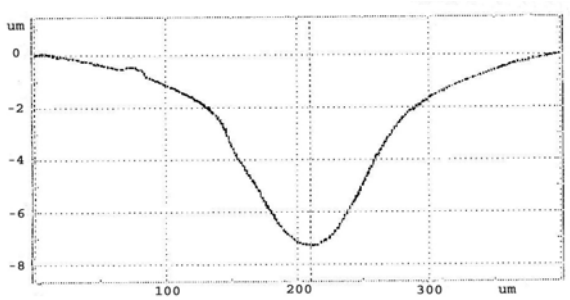

Figure 4. Surface profile over a dicing trench after PC3-6000 spinning. The PC3-6000 was bake at 200C for 5 minutes. 125μm deep cuts are planarized to within 7μm with this method.

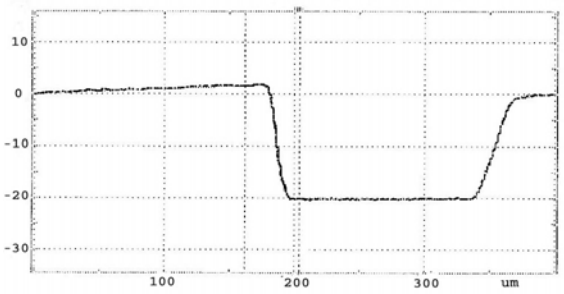

Figure 5 Surface profile over a dicing trench after PC3-6000 application. The PC3-6000 was baked at 200C for 5 minutes, then etched with oxygen to reveal the entire wafer surface. Note the final planarization is only to 20μm.

in an O_2 plasma until the surface of the wafer is entirely revealed. A surface profile of the resulting topography is shown in Fig. 5. As is shown, the final planarization is only approximately 20μm. Attempts to harden the PC3-6000 with UV radiation and/or fluorine ions failed to permit application of a second PC3-6000 layer without loosing the benefits of the original planarization.

2.3 Optical Flats

In search of an alternative method of planarization, we pursued a technique for replicating optical flats in interfacial sacrificial materials. Planarization by means of pressing a thermoplastic or thermosetting polymer between a device wafer and a flat superstrate was first proposed by Dill of IBM in 1984.[11] This method is related to a very old technique used to "polish" the surface of polymer-embedded specimens. Instead of laborious lapping and mechanical polishing of a block of cured thermoset polymer, a roughly lapped surface is "glued" to a glass plate (treated with a release compound) with the same polymer. Once the resin has cured, the block is separated from the glass. The previously lapped surface is then filled in with the polymer and the new surface replicates the polished glass plate. This technique was developed in 1993 by one of us (Bishop) using a polished sodium chloride disk as the planarizing superstrate and a low shrinkage epoxy resin as the sacrificial planarizing material.[12] Sodium chloride and potassium chloride (KCl) crystals are especially convenient for this work since they are easily dissolved in water. The general method of pressing and curing a thermoset resin against a wafer surface was also exploited by Prybyla in 1994 to aid in the planarization of silicon ULSI circuits.[13] The technology is used at the University of Virginia to fabricate air-bridged contacts for planar Schottky barrier diodes.[14,15]

Utilizing our method, a wafer with PC3-6000 is prepared and ramped to 160C in approximately 10 minutes. The wafer is then placed on a silicon carrier on a 200C hotplate for 5 minutes. The bubbles are then 'dragged' off of the wafer surface and the carrier/wafer is placed on a 160C hotplate for one minute. A KCl optically-flat crystal, that is ramped to 160C to avoid thermal shock, is then placed on top of the wafer and pressed with a 700g weight.[16] In order to avoid cracking of the PC3-6000, the assembly is slowly cooled to 40C in approximately 40 minutes. The crystal is then dissolved in water, and the 1 or 2μm of PC3-6000 remaining on the surface of the wafer is removed in an oxygen plasma. A surface profile over a dicing channel, as shown in Fig. 6, shows excellent planarization. We had previously realized that PC3-6000 thin films re-flowed when baked at 100C; however, it was found that intensive UV radiation of the PC3-6000 surface results in film stability up to 120C. Unfortunately, this thermal stability was not found for the much thicker films within the 125μm deep dicing channels. Fig. 7 is an SEM micrograph of a PC3-6000 planarized wafer after DC magnetron sputtering

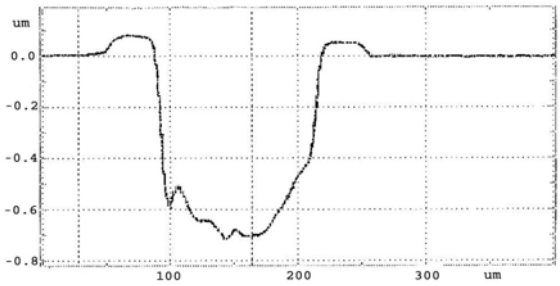

Figure 6. Surface profile over a dicing trench after PC3-6000 planarization with a KCl crystal and O_2 plasma etching. Au pads, on which to plate the beam-leads, are evident on both sides of the trench. Planarization in this case is within 700nm of the quartz.

of titanium (Ti) and Au. The excellent planarization of the channels is evident, but unfortunately the heat of the deposition process results in widespread cracking of the PC3-6000 film. Heat sinking of the wafer during the Ti/Au deposition avoids this problem. However, similar thermal cracking in the subsequent plating lithography process is unavoidable, even with increased UV exposures. The use of PC3-6000 with our KCl crystal press process is an excellent planarization method for smaller geometries (~10-20μm). However, it is unusable for our beam lead application. It may be possible to use the PC3-6000 process as the second step in a multi-planarization scheme, if the materials are chemically and thermally compatible.

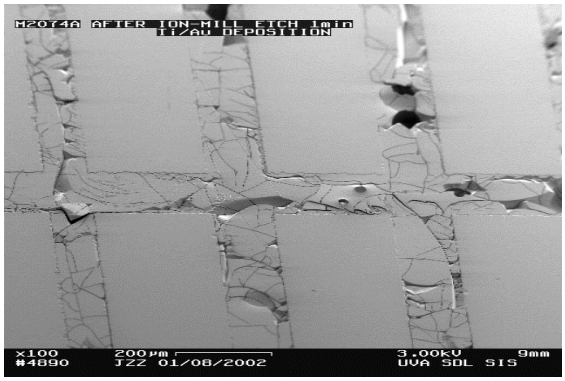

Figure 7. An SEM micrograph of a PC3-6000 filled, KCl planarized wafer after Ti/Au metallization. The PC3-6000 was thermally stressed during the deposition process.

It is clear that our method of using a KCl optical flat in combination with an appropriate sacrificial material is very promising. The remainder of this paper focuses on our search of appropriate materials for this process. The required properties of a suitable material are as follows: (1) sufficiently low viscosity when pressed with the KCl crystal, (2) thermal stability to 100C for subsequent lithography processing, (3) good adhesion to quartz, (4) good physical integrity for layers as thick as 150μm, (5) no trace inorganic content so that the material is etchable in an oxygen plasma, and (6) solvability in a liquid stripper, though the capability to remove the planarization material in the dicing avenues with an oxygen plasma is sufficient.

2.4 Waxes

We first investigated wax products for microscopy, lapping and dicing substrate mounting. Most of these materials soften well before 100C. However a mounting wax, 0CON-196 by Struers, Inc, was thermally stable well above 100C, had a relatively abrupt melting point around 157C to 162C and low viscosity above 165C.[17] Fig. 8 shows an SEM micrograph of a cross-sectioned wafer that has been planarized with a KCl crystal and the 0CON-196 wax. The wax in Fig. 8 was etched back to the quartz substrate with an oxygen plasma and has undergone Ti/Au metalization. The planarization is excellent. However, the wax adheres poorly to the quartz, and as a result, the wax pulls away from the dicing channels. Note that the wax is also cracked. The use of a Ti adhesion layer in the quartz channels did not improve the adhesion.

A number of different homopolymer materials were also investigated. Homopolymers, with more compact polymeric chains, typically have higher melting points and surface hardness. Most of these products, though, have a Mettler drop point well above 120C. They also soften significantly at 100C, resulting in cracking of the Ti/Au seed plating layer. Other polymers, such as maleated polypropylene, syndiotactic polystyrene, and linear polyethylene, with higher softening temperatures, had too high a melting temperature or too high a viscosity for beam lead processing. In our search for an appropriate material, we found epoxy resins are the best solution. We initially avoided these resins since they do not have a liquid stripper that is compatible with our circuitry materials. However, many of them are susceptible to an oxygen plasma and are therefore ultimately compatible with our process.

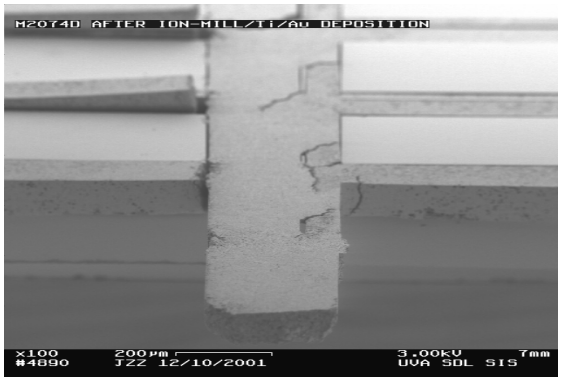

Figure 8. An SEM micrograph of a cross-sectioned wafer that has was planarized with a KCl crystal and the 0CON-196 wax. The planarization is excellent. However, the wax adheres poorly to the quartz, cracks and pulls away from the trenches.

2.5 Epoxy

The epoxy-based beam lead fabrication process is broken down into five sections for the sake of discussion. These are: trench dicing, planarization, beam plating, lapping and separation. Fig. 9 outlines these steps schematically. After fabrication of the mixer circuitry is complete, dicing cuts are made in the quartz substrate at the finished-chip boundaries. These cuts are made only partially through the wafer, essentially forming trenches in the quartz. The trenches are then filled with an epoxy resin, which is then planarized to the level of the quartz using an oxygen plasma. After the epoxy is planarized, Au pads are plated atop the quartz, overhanging the planarized, epoxy-filled trenches. The quartz substrate is then lapped from the backside to within the thickness of the trenches. Finally, the sacrificial epoxy is removed separating the individual chips from each other.

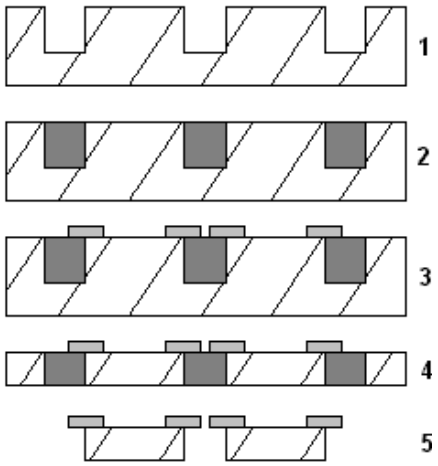

Figure 9. A basic outline of the beam lead fabrication process. The steps are (1) Trench Dicing, (2) Planarization, (3) Beam Plating, (4) Lapping and (5) Separation. Hatched areas represent quartz, while the dark gray and light gray regions represent the epoxy filler and Au beam leads, respectively.

2.5.1 Trench Dicing

After the SIS circuit fabrication process is complete, trenches are diced within, but not through the quartz along the perimeters of each of the individual chips. Fig. 10 shows an end-on photograph of three such trenches diced within a quartz substrate. Each trench requires multiple overlapping passes by the dicing saw in order to achieve the desired trench width. Trench depth is designed to be slightly larger than the final chip thickness; after the beam leads are fabricated, the quartz substrate is lapped from the back side, into the dicing channels, to the desired chip thickness.

Prior to dicing, a protective layer of AZP150 is spun over the quartz wafer.[18] Spinning is done at 6krpm for 30 seconds, resulting in a 1.4um thick film over the SIS circuitry. The protective coating is cured by baking at 100C for one minute. The AZP150 is similar to photoresist, but lacks the photoactive component. The coating serves to protect the SIS circuitry during the trench-cutting process by keeping slurry and other debris away from the SIS circuitry. Being a dielectric, the coating also helps prevent electrostatic discharge during the dicing process. After curing, the wafer is mounted, circuit side up, atop a four inch silicon carrier wafer. A thin layer of Apiezon W wax (black wax) is used to adhere the quartz wafer to the carrier.[19] The carrier is then mounted on the chuck of the dicing saw. For this work, we use a DAD-2H/6T automatic dicing saw, made by Disco, Co. The blade used in this work is a Disco NBC-ZH 2050 27HEDG. The blade produces a kerf width of between 50 and 60µm.[20] This kerf width, along with a 50% overlap between passes, results in a trench width of around 100µm. Trench depth is controlled by setting the saw blade to the appropriate height prior to initiating the cuts. For this work, trenches are cut 125µm deep.

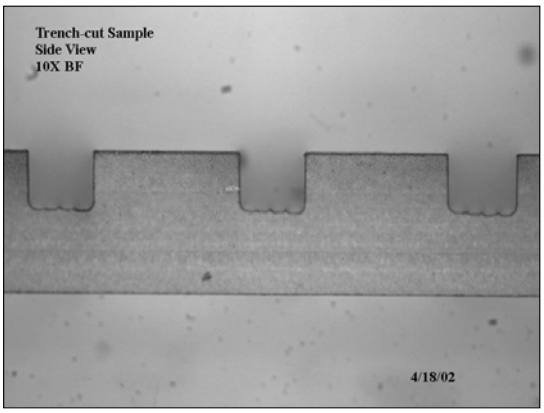

Figure 10. A photograph of the cross-section of three trenches cut into a quartz substrate. Trench widths are around 100µm. Using a 50% overlap between passes, each trench required four passes to achieve the desired width. Trench depth is around 125µm.

2.5.2 Planarization

After the trenches are diced, they are filled with a sacrificial epoxy resin. A crystal wafer, either KCL or NaCl, is then pressed atop the wafer, forcing the epoxy to cure such that it is planar along the top side of the quartz substrate. The epoxy is then etched back to the level of the quartz using an

oxygen plasma etch. With a planar interface between the quartz and epoxy, beam leads are then uniformly plated across the divide. Therefore, it is desirable to minimize any step height difference between the quartz and the epoxy to avoid a discontinuity in the beam lead structure at the interface.

For this work, we used a two part (10:1 resin to hardener ratio) epoxy made by Epoxy Technologies, Inc., known as Epo-Tek 330.[21] Epo-Tek 330 is a low viscosity, unfilled, 100% solids epoxy designed for bonding glass fiber optics. Epo-Tek 330 is relatively fast curing at low temperatures and has good wetting properties. The planarization process begins by preparing the epoxy resin in its appropriate ratio. For this work, we typically prepared small batches weighing 4.4 grams. The mixture is stirred vigorously for several minutes, then degassed in a vacuum desiccator for 35 minutes. This is done to drive out air bubbles that get trapped within the epoxy during mixing. Air bubbles trapped within the epoxy will prevent complete trench filling when poured over the trench-cut quartz substrate since such bubbles may not escape the trenches prior to complete curing of the epoxy.

While the epoxy is degassing, a NaCl or KCl crystal wafer is prepared. The crystal is used to press the epoxy firmly into the trenches of the quartz substrate during the curing of the epoxy. Once the epoxy is firmly cured, the crystal is removed from atop of the quartz substrate by dissolving it in de-ionized (DI) water. For this work, both KCl and NaCl crystals are used. No advantages are noted between the two as both serve equally well for the planarization process. The crystals are 50.8mm in diameter, 6mm thick and are optically polished on both sides. Preparation of the crystal begins by spin-cleaning with trichloroethane (TCA) and lightly scrubbing with a static-free swab. The crystal is then baked at 100C for 5 minutes in order to drive off excess solvents and moisture. Next, a polyimide layer is spun over the side of the crystal that is to contact the quartz substrate and epoxy. The polyimide layer serves to partially smooth out any abrasions that may exist on the crystal, thereby improving the planarization of the epoxy atop the quartz substrate. Also, the polyimide layer prevents the diffusion of salt into the epoxy resin during the curing process. It is suspected, though not conclusively shown, that salt contamination within the epoxy may impede the oxygen plasma etch process used to etch back the epoxy after curing. The OCG 286 polyimide used in this work must be cured at 160C for around 10 minutes on a hot plate after spin application. However, the non-uniform, rapid heating that occurs when a crystal is placed atop a 160C hot plate is enough to cause the crystal to crack. To avoid cracking, the crystal is incrementally heated by placing it on hotplates of 100C, 120C and 130C for one minute each prior to exposure to the 160C hotplate. This step-wise ramping is sufficient for heating the crystal slowly enough to avoid cracking. Likewise, once the crystal has been exposed to the 160C hotplate for 10 minutes, the process is reverse to allow the crystal to cool down slowly.

The trench-cut quartz substrate is then mounted atop a 2 inch silicon carrier with black wax. The carrier gives the wafer rigid support during the epoxy curing process and subsequent fabrications steps; the cured epoxy tends to impose a tensile stress on the quartz, which leads to cracking along the trench cuts where the quartz has been structurally weakened. After the epoxy is degassed and the quartz substrate is mounted atop the silicon carrier, the epoxy is gently dabbed onto the quartz substrate with a clean glass stir rod. The epoxy is then degasses for an additional 20 minutes, as small bubbles are often trapped within the epoxy during this application step. Following the final degassing, the silicon carrier (with the quartz substrate) and crystal are placed inside of a Teflon puck, with the crystal placed on top. The puck is designed to align the silicon carrier and the crystal atop one another during the curing process. The alignment prevents the crystal from sliding around atop the quartz substrate while the epoxy is curing. Teflon is used to avoid bonding the wafer/carrier to the puck. This puck assembly is then loaded into the body of a mounting press.[23] The press is used to impart 10psi of pressure atop the crystal, thereby pressing the crystal firmly against the quartz substrate. Fig. 11 shows a schematic diagram of the mounting press used for this work. The pressure induced by the

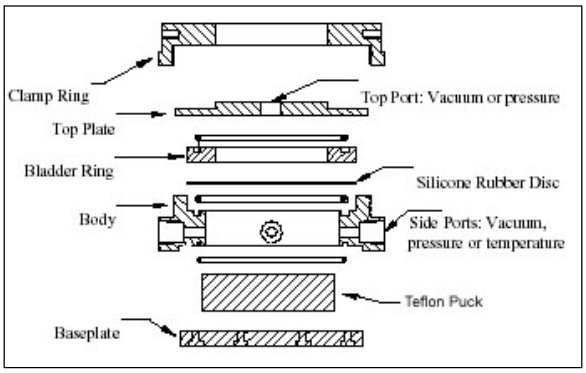

Figure 11. The UVa mounting press. The Teflon puck, which contains the crystal and quartz substrate, fits within the body of the press.[23]

mounting press onto the crystal ensures uniform planarization of the epoxy over the quartz surface. The entire assembly is place on a 95C hotplate for 3 hours. At this temperature, an internal temperature of 80C is slowly achieved within the press assembly. This extended period, low temperature, pressurized curing process ensures that the epoxy cures slowly within the trenches and without the quartz substrate experiencing excessive thermal expansion. This slow, low temperature curing process is critical for filling trenches uniformly, without voids.

After curing, the crystal is dissolved from atop the quartz substrate by exposure to a flowing stream of DI. Twenty minutes of exposure to a light flow of DI is sufficient to completely dissolve the crystal. After the crystal is removed, the epoxy is etched back to the level of the quartz. The pressing of the crystal against the quartz substrate creates a nearly uniform layer of epoxy that is around 10 to 15μm thick. The etch-back process is used to remove this excess epoxy from the wafer until the epoxy in the trenches is nearly level with the quartz surface. During this process, the polyimide is also removed. A tolerance of around 1 to 2μm is acceptable, as the 10μm Au plating thickness is enough to provide rigid support to the beam leads despite such a slight mismatch. The epoxy is etched back using an oxygen plasma etcher. Power is set at 200W and pressure is set to 1Torr. The etch-back process is monitored visually and terminated when the epoxy is removed from atop the open fields of the quartz. This etch-back process takes around 45 minutes to complete. An increase in power to the plasma etcher would increase the etch rate. However, in order to maintain the process requirement that temperatures not exceed 200C for significant time periods, increasing the power of the etch is not desirable.

2.5.3 Plating

After planarization, a plating seed layer is sputtered over the wafer. The seed layer consists of 15nm of Ti below 50nm of Au. The Ti serves as an adhesion layer for the Au plating seed. The Ti and Au are deposited consecutively in a multi-target sputtering system using DC magnetron sputtering. System base pressure is ~$3x10^{-8}$ Torr. Prior to metal deposition, the quartz substrate is lightly cleaned with an ion mill. The ion mill rids the quartz substrate of moisture and lightly roughens the surface prior to sputtering. The effect is to increase adhesion between the plating seed layer and the quartz/epoxy surfaces.

Prior to plating, features are patterned using a thick (13μm) resist. The resist used in this work is AZ4903.[18] Special care must be taken to ensure the resist does not crack, bubble or re-flow during the lithography process nor during subsequent fabrication steps. Prior to resist spinning, the wafer is pre-cleaned with ethanol, TCA and methanol. This is followed by an ozone exposure and a 120C hot plate bake. The wafer is then treated with hexamethyldisilazane (HMDS) in order to promote resist adhesion to the seed layer. The resist is spun at 2.5krpm for 30 seconds in a vapor of propylene glycol monomethyl ether acetate (PGMEA). The resist is then allowed to sit for 35 minutes prior to soft baking at 120C for 90 seconds. Pausing prior to soft baking allows solvents in the resist to evaporate more slowly, preventing the resist from bubbling during the soft bake process. Spinning of AZ4903 at 2.5krpm leaves a significant edge bead that must be removed prior to pattern exposure to ensure conformal contact between the wafer and the lithography mask. Exposure is done using a 320nm (broadband) wavelength, deep ultra-violate (DUV) contact aligner. The resist is exposed for 10 minutes, then developed in AZ400k (diluted 1:4) for roughly 4 minutes. Fig. 12 shows a top-down photograph of two chips after the plating lithography process is complete. The light gray areas are not covered with resist. These are the regions where Au plating will occur. Note that these open areas overlap both the quartz (smooth regions of the chips) and the epoxy-filled trenches (rough areas between the chips).

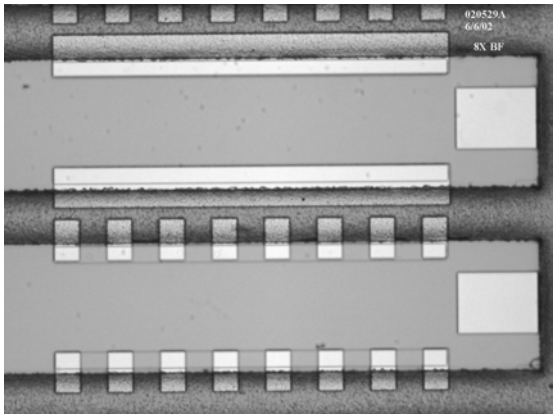

Figure 12. A photograph of quartz chips (smooth regions) surrounded by epoxy-filled trenches (rough regions). The plating lithography patterns overlap the quartz and epoxy, allowing Au beam leads to be plated across the interface. Two different beam lead patterns are shown here.

Following patterning, the resist thickness is measured using a profilometer. The wafer is then mounted onto a small plating jig using a low melting point wax; exposing the wafer to temperatures in excess of 110C will cause the resist to re-flow, thereby ruining the lithographic pattern. The plating solution used in this work is Technic 25E.[22] The solution is heated to 50C in a DI bath. Plating current is set to 10mA, giving a plating rate of around 500nm per minute. Note that this plating rate is dependant on exposed wafer area as well as the plating current. Plating progress is monitored incrementally every four or five minutes using the profilometer until the desired 10µm of plated Au is achieved. Following plating, the AZ4903 resist is removed with a light acetone spray. Finally, the un-plated regions of the seed layer are removed using a series of wet etchants. The Au is removed using an iodine-based solution in ethanol. This is followed by the removal of the Ti in a 10:1 solution of buffered oxide etchant (BOE). Fig. 13 shows an SEM micrograph of a beam lead after the resist and seed layers are removed. The beam lead extends out from the quartz chip in the lower left of the image, over the epoxy-filled trench in the upper right.

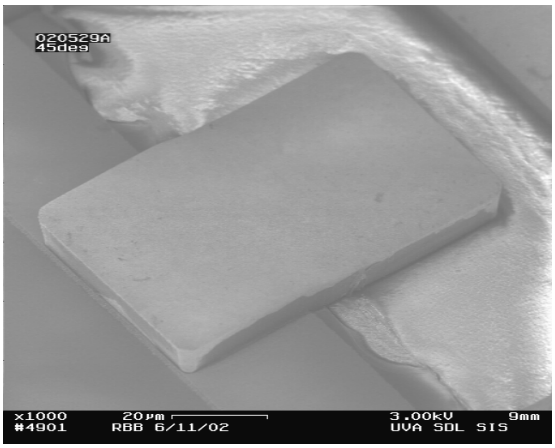

Figure 13. An SEM micrograph of an Au beam lead. The 10µm thick Au structure extends from the quartz chip (lower left, dark) over the epoxy-filled trench (upper right, bright).

2.5.4 Lapping

After plating is complete, the quartz substrate is mounted onto a two inch silicon carrier, with the bottom side of the quartz wafer (non-device side) exposed. The quartz substrate is adhered to the silicon carrier using black wax. The carrier wafer, with the quartz substrate, is then placed onto a lapping system mounting disc, again using black wax. Essential to achieving uniformly thinned chips is starting with a quartz substrate that is level with respect to the silicon carrier wafer. To achieve this, the mounting disc and the carrier wafer are placed in the mounting press. The press is then placed on a hot plate and a pressure of 10psi is applied to the carrier and disc. The press is left on the hot plate until an internal temperature of 130C is achieved and held for 5 minutes. At 130C, the black wax melts, allowing the quartz substrate and the silicon wafer to be pressed firmly together. The mounting press is then removed and allowed to cool on a Peltier prior to removing the 10psi of pressure. Once the mounting press has cooled to room temperature, the pressure is released, leaving the quartz substrate, silicon carrier and mounting disc uniformly pressed together.[23]

The mounting disc is then fitted onto the arm of an AHTP Mutliprep lapping system. This particular lapping system has a specific parallelism of +/- 2µm over a diameter of 2.25 inches. The backside of the quartz substrate is then thinned using a 30µm grit lapping film. After lapping away approximately 75% of the desired quartz, the 30µm lapping film is removed. The remaining quartz is lapped using 15µm grit lapping film, which leaves a smoother finish on the back side of the quartz chips.

2.5.5 Separation

After the backside of the quartz is lapped down to within the depth of the epoxy-filled trenches, the epoxy between the chips is removed. This is done by using an oxygen plasma etch process, with conditions identical to those used to etch back the epoxy after the curing process. An exposure to the oxygen plasma of around 40 minutes is sufficient for removing all of the remaining epoxy between the chips. Once the epoxy is removed, the individual chips are separated from the silicon carrier by rinsing in a beaker of TCA. The chips are then removed from the TCA by filtering through a small piece of filter paper. Individual chips are then separated by picking through the lot with a pair of tweezers. Fig. 14 is an SEM micrograph of two quartz chips with completed beam leads. A close-up of one of the small beam lead structures is depicted in the SEM micrograph shown in Fig. 15.

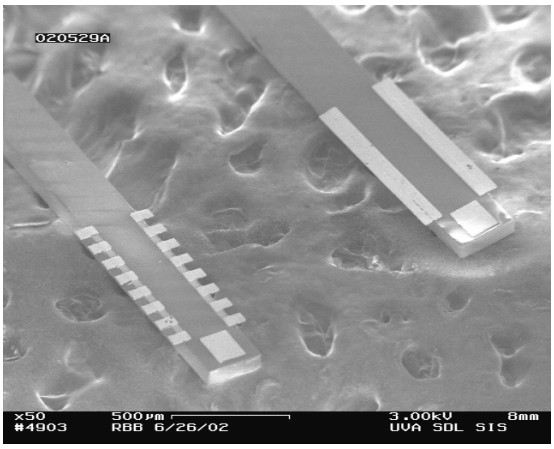

Figure 14. An SEM micrograph of two separated chips with completed beam leads.

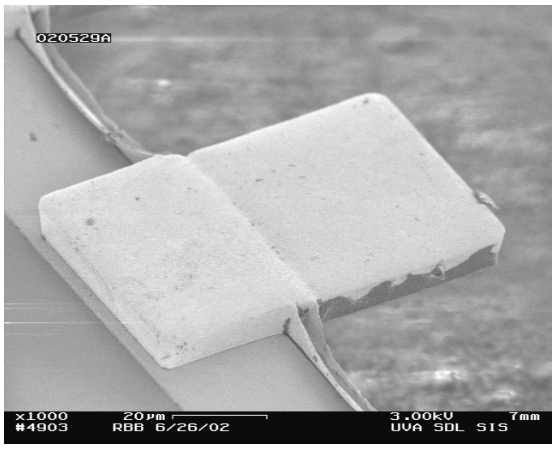

Figure 15. An SEM micrograph of a completed beam lead. The 10µm thick, Au beam lead is extending out from the quartz chip located in the lower left.

3. CONCLUSION

We have successfully demonstrated the ability to fabricate Au beam lead structures on quartz substrates. The fabrication constraints defined by quartz, as well as those imposed by the materials comprising the Nb-based SIS circuitry, present unique processing problems for the fabrication of Au beam leads on quartz substrates. Through the use of quartz trench dicing, planarization of epoxy resins within the trenches, and platting of Au structures across the quartz/epoxy interface, our group has shown this technology is a viable option for integration into quartz-based SIS circuitry. This technology will enhance the assembly of superconducting millimeter and submillimeter-wave circuits, especially for applications requiring smaller chip dimensions and tighter design tolerances. Integration of beam lead technology with Nb-based superconducting millimeter and submillimeter waveguide circuit fabrication will also help meet the throughput requirements of large, and demanding, radio astronomy projects.

We would like to note that, despite the successes mentioned in this paper, the beam lead fabrication process is not yet fully optimized. Issues still remain regarding our process, including improving device yields and maintaining processing temperatures below 200C. The device yields currently are encouraging, approximately 40%, for the long beam lead structures pictured in the upper right of Fig. 14. Yields are lower for the more complicated, multiple beam lead chips pictured in the lower left of Fig. 14; this may be attributed largely to the separation process, which places a considerable stress on the beam leads as they are rinsed off of the carrier wafer with TCA and then handled with tweezers. The beam leads have a tendency to break off if they are handled too roughly. Maintaining processing temperatures below 200C is also still a concern; the epoxy plasma etch process imparts a large amount of energy to the wafer, which is converted to heat within the quartz substrate. We are still not quite sure how hot these wafers are getting during the 200W oxygen plasma etch. Maintaining low processing temperatures is critical to fabricating beam leads on circuits containing SIS junction, especially considering the tendency of the SIS aluminum barrier layer to oxidize when exposed to excess heat for long periods of time. We have yet to integrate beam leads onto quartz chips containing SIS devices and Nb circuitry. As a result, we do not yet have a full understanding of the impact that beam lead processing has on the characteristics of superconducting millimeter and submillimeter waveguide circuits.

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